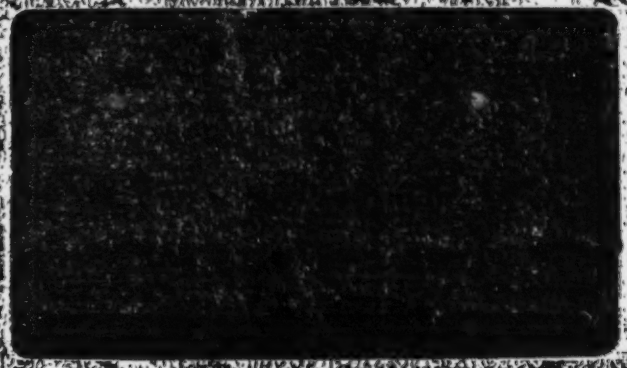
89-651



MCS MILLER COMMUNICATIONS SYSTEMS LTD.

DIGITAL RECEIVER
SYSTEM STUDY

FINAL REPORT

MCS File No.: DREO-04

DREO File No.: W7714-8-5638

DSS Contract No.: 660ER-7-0003/96

Date: March 27, 1989

Prepared By: John Bodie

J. Bodie

MCS MILLER COMMUNICATIONS SYSTEMS LTD.

300 Legget D
Kanata, Ontu
Canada K2K

Table of Contents

1.0 INTRODUCTION 1
1.1 Background 1

2.0 SYSTEM REQUIREMENTS 3
2.1 Frequency Domain Requirements 3
2.2 Time Domain Requirements 3
2.3 Amplitude Domain Requirements 3
2.3.1 Instantaneous Dynamic Range 4
2.3.2 Spurious-Free Dynamic Range 5
2.3.3 Instantaneous Spurious-Free Dynamic Range 5
2.4 Operational Requirements 6

3.0 SYSTEM ARCHITECTURES 7
3.1 Observation Bandwidth 7
3.1.1 Normal Resolution 7
3.1.2 Variable Resolution 8
3.2 RF Digitization 8
3.2.1 Partial-band RF Digitization 9
3.3 IF Digitization 9
3.4 Baseband Digitization 9
3.5 Candidate Architectures 10
3.5.1 RF Architecture 11
3.5.2 Wide-IF Architecture 11
3.5.3 Mid-IF Architecture 11
3.5.4 Narrow-IF Architecture 12

4.0 ANALOG PROCESSING 13
4.1 Performance Requirements 13
4.2 System Gain 14
4.2.1 AGC 14
4.3 Baseline Front-End Design 15
4.3.1 Frequency Plan 15
4.3.1.1 RF Architecture 16
4.3.1.2 Wide-IF Architecture 16
4.3.1.3 Mid-IF Architecture 17
4.3.1.4 Narrow-IF Architecture 18
4.3.2 Performance 18

5.0 A/D CONVERSION 19
5.1 Design Relationships 19
5.1.1 Quantizing Noise 19
5.1.2 Aperture Uncertainty 20
5.1.3 Linearity 21
5.1.3.1 Second-Order Products 21
5.1.3.2 Third-Order Products 22
5.1.3.3 Applicability 22
5.2 Component Performance 22
5.3 Implementation Considerations 23

6.0	DIGITAL PROCESSING	26
6.1	Design Relationships	26
6.1.1	Windowing	26
6.1.2	Computational Requirements	27
6.1.3	Block Size	28
6.1.4	Processing Speed	28
6.2	Component Performance	29
6.2.1	Program Memory	29
6.2.2	Data Memory	29
6.2.3	Processor	30
7.0	SYSTEM SELECTION	31
7.1	Architecture Evaluation	31
7.2	Architecture Selection	32
7.3	Processing Architecture	32
8.0	PERFORMANCE ANALYSIS	34
8.1	Signal Processing Performance	34
8.1.1	Dynamic Range	34
8.1.2	Frequency Range	34
8.1.3	Frequency Resolution	34
8.1.4	Observation Rate	34
8.2	Probabilistic Performance	35
8.2.1	Probability of Interception	35
8.2.2	Detection Criterion	35
8.2.3	Probability of Detection and of False Alarm	35
8.2.4	Effect of Averaging	35
9.0	RECOMMENDATIONS	37
9.1	Implementation Estimates	37
9.2	Further Work	37
10.0	REFERENCES	38

List of Figures

3.1	Receiver Architectures	7.1
3.2	IF Architecture Sampling Frequency Plan	11.1
3.3	RF Architecture Sampling Frequency Plan (Fs = 264 MHz)	11.2
3.4	RF Architecture Sampling Frequency Plan (Fs = 220 MHz)	11.3
5.1	Quantizing Noise	19.1
5.2	Quantizing Noise Power Spectrum	19.2
5.3	Quantizing Noise Power Spectrum (AWGN = 1 LSB)	19.3
5.4	Quantizing Noise Power Spectrum (AWGN = 1/2 LSB)	20.1
5.5	Quantizing Noise Power Spectrum (AWGN = 1/4 LSB)	20.2
5.6	Quantizing Noise Power Spectrum (AWGN = 1/8 LSB)	20.3
5.7	Quantizing Noise Power Spectrum (Dither = 1 LSB)	20.4
5.8	Quantizing Noise Power Spectrum (Dither = 1/2 LSB)	20.5
5.9	Quantizing Noise Power Spectrum (Dither = 10 LSB)	20.6
5.10	A/D Converter Harmonic Distortion	22.1
5.11	A/D Converter Performance	22.2
6.1	Window Function	27.1
6.2	Window Spectral Response	27.2
6.3	Digital Signal Procesor Performance	30.1
9.1	Receiver Block Diagram	37.2

List of Tables

4.1	RF Amplifier Performance	13.1
4.2	Frequency Conversion Products (Wide-IF 1st Conversion)	16.1
4.3	Frequency Conversion Products (Wide-IF 2nd Conversion)	17.1
4.4	Frequency Conversion Products (Mid-IF 2nd Conversion)	18.1
4.5	RF Architecture Front-End Design	18.5
4.6	IF Architecture Front-End Design	18.6
7.1	Architecture Evaluation Parameters	31.1
9.1	Implementation Estimates	37.1

1.0 INTRODUCTION

This report evaluates the performance tradeoffs which influence the design and construction of hybrid analog/digital wideband Communications ESM surveillance receivers. The receivers considered are based on conventional electronic signal processing techniques, as opposed to non-electronic technologies such as SAW or acousto-optic devices. Operation in the surveillance/intercept mode is of prime concern, although some consideration is given to the applicability of the receivers to signal analysis functions.

A set of receiver architectures is defined, each reflecting a different location of the analog/digital boundary. The performance of each receiver subsystem is analyzed, and the results used to define candidate systems of differing architectures. The overall performance of the candidate systems is evaluated, and an optimal system selected. The performance of the selected system is analyzed in detail.

An estimate is provided of the cost of implementing the selected system, and recommendations are made for further work.

1.1 Background

The purpose of a Communications ESM receiver system is to monitor the frequency spectrum over a predefined range and to provide as much information as possible about any signals present. This involves two basic functions: spectral surveillance, which detects signal activity, and signal analysis, which yields information on the signals detected. The two functions are normally performed in separate modes of operation, or by totally separate receivers.

During spectral surveillance, processing is performed over the entire frequency range of interest, although not necessarily at all frequencies simultaneously.

During signal analysis, the receiver is normally tuned to a selected signal and the processing performed only over the bandwidth of that signal. The analysis can involve demodulation of the message carried by the signal, spectral analysis, signal fingerprinting, or more sophisticated functions such as call sign recognition or language recognition and translation.

The primary requirements for a Communications ESM receiver performing spectral surveillance are a wide dynamic range (in excess of 100 dB) and a probability of interception approaching 100%, even for short-duration signals such as frequency hopping and burst transmissions. The overall frequency range of interest for tactical land EW operations is from 0.5 to 4000 MHz, although the VHF band (30 to 88 MHz) is of prime importance. The receiver frequency resolution should be variable, with a minimum resolution of as low as 100 Hz to allow the separation of CW-OOK (on/off keying) transmissions.

Conventional surveillance systems are typically of the superheterodyne type, with the narrowband version the most common. The narrowband receiver is tuned to a single channel at any one time, and covers the frequency range of interest by stepping or sweeping between channels. The signal processing is normally analog, with any digital signal processing performed at baseband using the output of an energy detector for the selected channel. This type of receiver offers high sensitivity and wide dynamic range, but suffers from a fundamental trade-off between frequency resolution and probability of interception.

The wideband superheterodyne receiver improves the probability of interception by observing a group of channels simultaneously within a wider IF bandwidth. The required bank of channel filters can be implemented efficiently by digitizing the IF signal and performing a real-time Fast Fourier Transform. Other advantages of using digital signal processing at the IF stage of the receiver include increased system flexibility, precisely controlled filter characteristics, and improved quadrature phase accuracy. However, the dynamic range of this type of receiver is generally less than that of a narrowband receiver, due to the achievable resolution and linearity of high-speed A/D converters.

One approach to implementing a wideband superheterodyne receiver is to use the front end (e.g., from RF input to first IF output) of an existing narrowband receiver, followed by digitization and digital processing. However, in this case intermodulation products or other spurious signals that would normally be rejected by the single channel filter may appear in the digital output. To ensure optimal performance, it is necessary to design the receiver front end under the constraint that the entire IF bandwidth (or a major part of it) will be processed simultaneously.

2.0 SYSTEM REQUIREMENTS

This section identifies the performance parameters that are of interest, and the overall requirements which the receiver is intended to meet. The primary application envisaged is the interception and potentially the demodulation of frequency-hopping tactical radio transmissions.

2.1 Frequency Domain Requirements

The frequency band of interest is VHF, 30 to 88 MHz. The receiver should be capable of resolving signals separated by no more than the bandwidth of the target transmissions, typically 25 kHz.

It is also desirable that the receiver be capable of variable frequency resolution, to a minimum of 100 Hz. In this mode, the time-domain requirements specified below need not be met.

2.2 Time Domain Requirements

A single-hop probability of interception of close to 100% is desired. This requires that each frequency bin in the coverage range be observed no less frequently than the hopping rate of the target transmissions, typically 100/sec.

2.3 Amplitude Domain Requirements

The amplitude domain requirements result from the need to detect signals in the presence of receiver noise and of other signals, and to distinguish between received signals and spurious signals generated internally by the receiver.

Two main amplitude domain requirements can be defined: minimum discernible signal (MDS) and dynamic range.

The MDS represents the lowest-level input signal that can just be distinguished from the receiver noise floor. An MDS of -120 dBm or less in a 25 kHz bandwidth is desired, corresponding to a noise figure of 10 dB.

Note: there is no universally accepted quantitative definition of the MDS. In this report, the MDS is defined as the power of the broadband noise floor within the detection bandwidth, referred to the receiver input.

The dynamic range of the receiver represents the difference in level between the largest and smallest signals for which the receiver operates satisfactorily according to some criterion. A dynamic range of 100 dB or greater is desired.

For the purpose of this report, three types of dynamic range are defined:

1) Instantaneous dynamic range (DR_I)
2) Spurious-free dynamic range (DR_S)
3) Instantaneous spurious-free dynamic range (DR_{SI})

The instantaneous dynamic range is defined as the largest difference (in dB) between the levels of two simultaneously applied input signals for which the receiver is still able to detect the presence of the lower power signal. This indicates the ability of the receiver to process signals of widely differing power levels simultaneously.

The spurious-free dynamic range is defined as the range of input signal levels between the minimum discernible signal (MDS) and the level for which the third-order intermodulation products, referred to the input, exceed the MDS. This indicates the range of signal levels over which the receiver can operate without introducing false signals.

The instantaneous spurious-free dynamic range combines the requirements of the two previous definitions. It is defined in the same manner as the DR_S, except that the MDS is determined by applying a low-level test signal simultaneously with the high-level signals that give rise to the intermodulation products. This indicates the ability of the receiver to process signals of differing power levels simultaneously without introducing false signals, and appears to be the most meaningful measure of amplitude-related performance for a wideband receiver.

2.3.1 Instantaneous Dynamic Range

For an ideal fixed-gain receiver, the instantaneous dynamic range is infinite, as the level of the larger signal does not affect the detectability of the smaller. In practice, the instantaneous dynamic range is limited by factors such as:

1) Finite filter stop-band attenuation - the larger signal can leak through the detection bandwidth filter and mask the presence of the smaller signal.

2) Desensitization - when limiting is experienced (e.g., in an amplifier or mixer), the output level of the smaller signal is reduced as the input level of the larger signal increases, and can eventually drop below the noise floor.

3) Reciprocal mixing - the larger signal can mix local oscillator phase noise into the detection bandwidth of the smaller signal, thus raising the noise floor.

With AGC, the larger signal can cause the gain to be reduced to the point where the smaller signal is below the MDS, thus limiting the instantaneous dynamic range.

Note that for this definition of instantaneous dynamic range, the highest signal level that can be accommodated is limited only by the possibility of physical damage or receiver malfunction. This is in contrast to the case of a measuring receiver, where an upper limit is established at the point where gain compression prevents accurate level measurement. Such a limit (e.g., the 1 dB compression point) could also be applied to the present case.

2.3.2 Spurious-Free Dynamic Range

For a fixed-gain receiver, the spurious-free dynamic range is determined by the third-order intercept point, the noise figure, and the detection bandwidth, as follows:

$$DR_S = \frac{2}{3}[\, IP3i - (No + NF + BW)\,] \quad [dB]$$

where

IP3i = third-order input intercept point
No = thermal noise density
(-174 dBm/Hz @ 50Ω)
NF = receiver noise figure [dB]
BW = detection bandwidth [dBHz] (= 10 log B [Hz])

The use of AGC can extend the spurious-free dynamic range by increasing the maximum level that can be applied without generating detectable third-order products. If the AGC is applied by means of an attenuator at the receiver input, any desired DR_S can be achieved. If the AGC is applied later in the processing chain, the overall DR_S will not exceed that of the elements preceding the attenuator.

2.3.3 Instantaneous Spurious-Free Dynamic Range

Neither DR_I nor DR_S as defined above is entirely satisfactory as a measure of performance for a wideband surveillance receiver, as both values can be unrealistically high. The definition of DR_I ignores the possible presence of detectable spurious signals, while the value of DR_S can be increased arbitrarily by applying AGC at the receiver input.

In actual operation, the receiver is required to detect small signals in the presence of large, without introducing false signals due to spurious products. The definition of DR_{SI} provides a direct measure of this ability, and gives a result which is independent of AGC at the receiver input.

The DR_{SI} can be measured by applying two equal signals and increasing their level until discernible spurious products appear, and then applying a third input signal at the level required to produce a discernible output signal. The difference between the high and low input levels gives the DR_{SI}.

Depending on the threshold at which AGC is applied, it may not be possible to evoke discernible spurious products. In this case, the MDS can be measured as a function of the level of the high-level test signals, and the DR_{SI} taken as the largest difference between the two.

For a component or system where the noise floor is independent of the input level, DR_{SI} is equivalent to DR_S.

2.4 Operational Requirements

The system should satisfy the following general operational requirements:

1) Flexible selection of parameters, including:
   - frequency range
   - frequency resolution
   - observation time
   - detection criteria
   - lock-out frequencies

2) Convenient display of detected signal parameters

3) Efficient transition or hand-off between surveillance and analysis modes.

3.0 SYSTEM ARCHITECTURES

Figure 3.1 shows the general receiver architecture considered. The receiver consists of an input bandpass filter and RF amplifier, followed by a series of frequency conversion (IF) stages. Each conversion stage consists of a mixer and its associated local oscillator, followed by an IF bandpass filter and amplifier. The final IF stage is followed by an energy detector and an averaging filter.

The number of IF stages used is determined by the input frequency range to be covered, the IF bandwidth desired, and the degree of suppression of spurious signals such as image frequencies and intermodulation products that is required. For the VHF band, double or triple conversion would normally be used.

Digitization can be performed at RF, at any of the IFs, or at baseband. It may be desirable to digitize at more than one point: for example, at RF to allow the fastest observation of the full band, and at IF to provide finer frequency resolution over a reduced bandwidth.

AGC is not shown in the receiver architecture, but can be modelled as a variable attenuator at one or more points in the signal flow. The effects of AGC are considered in section 4.2.

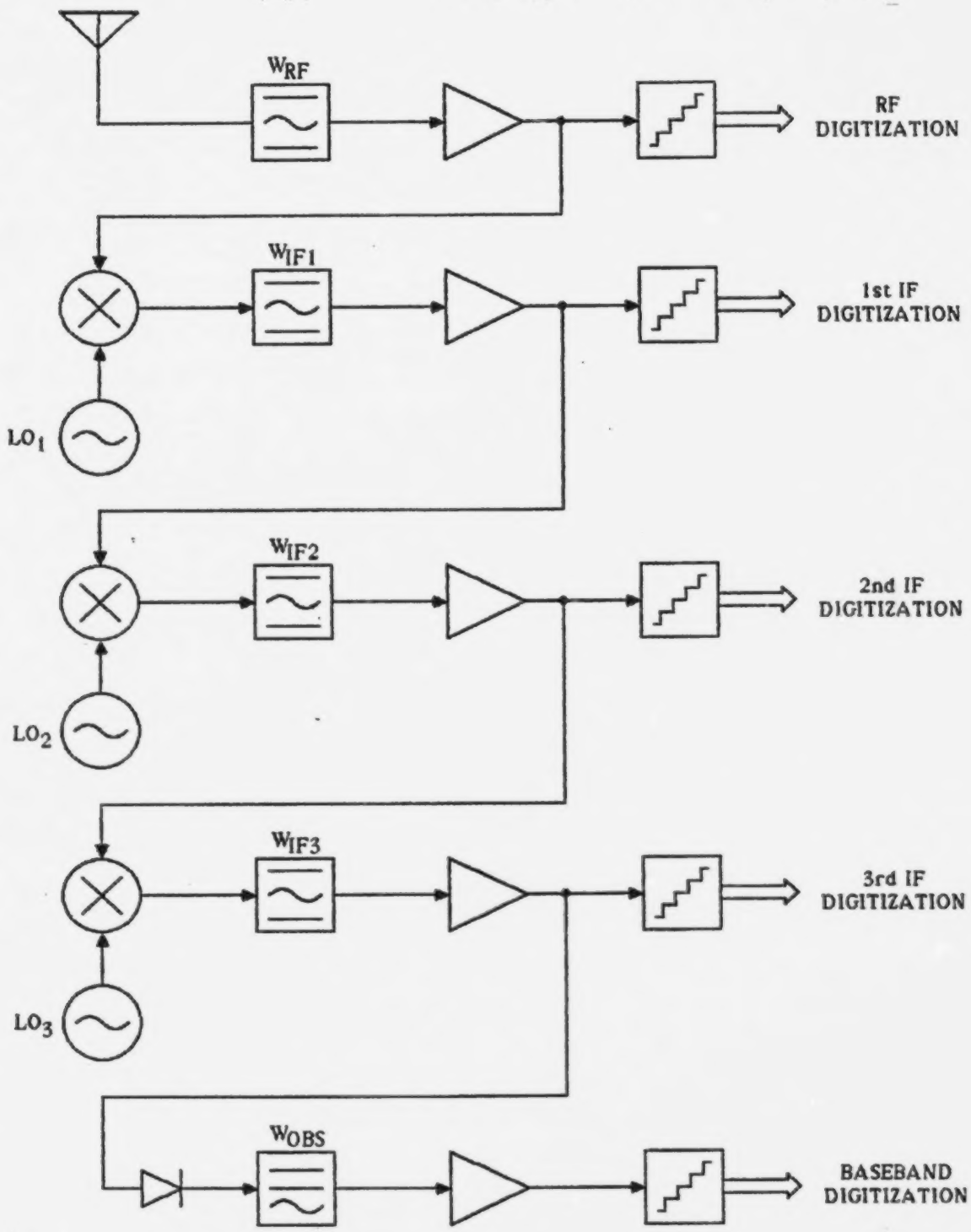
3.1 Observation Bandwidth

The choice of architecture is determined primarily by the observation bandwidth that is required, where this is defined as the bandwidth within which all channels are observed simultaneously. The period for which the observation bandwidth is observed determines the frequency resolution that can be obtained in subsequent processing of the digitized samples.

3.1.1 Normal Resolution

As noted in sections 2.1 and 2.2, the fundamental performance requirement of the receiver is to observe each 25 kHz channel in a 58 MHz bandwidth at least once every 10 ms. This requirement can be met for a range of processing bandwidths. For any processing bandwidth less than the full coverage range, the receiver must scan: that is, observe segments of the coverage range sequentially.

The resolution requirement of 25 kHz implies a minimum observation time of 40 μs, corresponding to an FFT bin size of 25 kHz. However, to avoid spurious responses due to the sidelobes of the bandpass filters implemented via the FFT, it is necessary to employ a finer frequency resolution. As discussed in section 6.1.1, a resolution of 8 FFT bins per channel will provide good performance. This yields a bin size of 25/8 = 3.125 kHz and a minimum observation time of 320 μs.


W_RF
RF DIGITIZATION
W_IF1
1st IF DIGITIZATION
LO_1
W_IF2
2nd IF DIGITIZATION
LO_2
W_IF3
3rd IF DIGITIZATION
LO_3
W_OBS
BASEBAND DIGITIZATION

The requirement to observe each channel at least every 10 ms limits the maximum number of sequential observations to 10 ms/320 μs = 31. This requires an observation bandwidth of at least 58 MHz/31 = 1.87 MHz, or approximately 75 channels. The need to observe multiple channels simultaneously to meet the basic performance requirement implies that a wideband architecture must be used.

Any observation bandwidth greater than the minimum can also be used. With a larger bandwidth, fewer sequential observations are required to encompass the full coverage range, and hence each channel can be observed more frequently. Alternatively, the resolution can be improved by increasing the observation time, while maintaining the channel observation rate.

For a given frequency resolution and channel observation rate, the digital processing computational requirements increase with increasing observation bandwidth. This is discussed further in section 6.1.

3.1.2 Variable Resolution

For any observation bandwidth, the frequency resolution can be improved by increasing the observation time. If it is not necessary to maintain a given channel observation rate, the limiting factor in determining the achievable resolution is likely to be the maximum FFT block size that can be accommodated.

For example, for a maximum block size of 2^{16} and digitization at a rate of 264 MHz, corresponding to an observation bandwidth of 88 MHz at 1.5 times the Nyquist rate, the frequency resolution would be $264/2^{16} \approx 4$ kHz. To achieve 100 Hz resolution with this block size, the sampling rate would be limited to 6.6 MHz, which would allow an observation bandwidth of about 2.2 MHz.

3.2 RF Digitization

RF digitization allows the entire coverage band to be processed simultaneously, providing continuous surveillance at all frequencies. It also eliminates the need for mixers, local oscillators, and IF amplifiers, all of which can introduce performance degradations. However, it makes the greatest demands of the A/D conversion and digital processing elements.

The feasibility of RF digitization is dependent on the coverage bandwidth, which determines the sampling rate and processing speed required, and on the absolute RF frequency, which determines the maximum acceptable sampling aperture uncertainty.

For the VHF band (30 to 88 MHz), the bandwidth is 58 MHz, which requires a theoretical sampling rate of 116 MHz. In practice, a rate of 1.5 to 2 times the Nyquist rate would be used, corresponding to approximately 175 to 230 MHz. The additional complexity of complex bandpass sampling can be avoided by sampling the entire DC to 88 MHz band, at a rate of approximately 250 to 350 MHz.

As discussed in Section 5.1.2, the required aperture uncertainty would be on the order of 5 ps.

3.2.1 Partial-band RF Digitization

Rather than digitizing the full RF band, it can be split into a number of sub-bands using a bank of bandpass filters. The partial bands can be digitized in parallel, or scanned sequentially.

The parallel approach retains the advantage of continuous surveillance of the entire band, while reducing the sampling rate required. The total computational requirement is reduced slightly from that for full-band digitization, as FFT complexity decreases slightly faster than linearly with decreasing block size.

The sequential approach reduces the sampling rate and the computational requirement, at the expense of continuous full-band surveillance. It is equivalent to IF digitization with a fairly wide IF bandwidth, except that it retains the advantage of eliminating the frequency conversion components.

3.3 IF Digitization

With IF digitization, only a portion of the coverage band is observed at one time. As for partial-band RF digitization, this reduces the sampling rate and processing speed requirements, but precludes continuous full-band surveillance. As discussed in section 3.1, however, this need not prevent the receiver from meeting the overall performance requirements, as long as the IF bandwidth is sufficient. For the purpose of this study, the IF bandwidth will be assumed to be at least equal to the minimum observation bandwidth derived above.

It is possible for the entire RF coverage bandwidth to be translated to IF as a block. In a situation where the absolute RF frequency is large compared to the coverage bandwidth, this approach retains the advantage of full-band digitization while relaxing the A/D aperture uncertainty requirement. For the VHF band, however, it does not provide a significant benefit. For the purpose of this study, the IF bandwidth will be assumed to be substantially smaller than the RF bandwidth.

3.4 Baseband Digitization

Baseband digitization is shown as following an energy detector, and hence the digitized signal cannot be analyzed to separate individual channels within the baseband. This configuration represents the narrow-band superheterodyne architecture, which is not of interest for this study.

Rather than using an energy detector, it is possible to convert to baseband using quadrature LOs. This results in a complex baseband representation of the signal, which can be digitized in separate I and Q channels and further analyzed. This is

conceptually equivalent to IF digitization, but introduces additional complexity. It has the advantage that the A/D conversion is performed on a signal of lower frequency, which reduces the demands on the sample-and-hold device.

3.5 Candidate Architectures

For the purpose of this report, we will consider the following candidate architectures:

1) RF digitization over the range DC to 88 MHz. This architecture is the simplest with respect to the analog front-end, and offers the possibility of continuous observation of all channels within the entire coverage band. It will be referred to as the "RF" architecture.

2) IF digitization with an observation bandwidth of approximately one-tenth the coverage range. This architecture is convenient for comparison with RF digitization in terms of performance and of implementation complexity. As shown in section 5.2, this is also roughly the maximum observation bandwidth for which present-day A/D converters can approach the target of 100 dB dynamic range for signals of 25 kHz bandwidth. It will be referred to as the "Wide-IF" architecture.

3) IF digitization with the minimum observation bandwidth that allows a channel observation rate of 100 Hz to be achieved. This architecture minimizes the demands on the A/D converter and the digital processing elements. It will be referred to as the "Mid-IF" architecture.

4) IF digitization with the maximum observation bandwidth that allows 100 Hz channel resolution to be obtained with an FFT of reasonable size. This will be referred to as the "Narrow-IF" architecture.

   Note: the Narrow-IF architecture provides the fine frequency resolution required for channels narrower than 25 kHz, but does not satisfy the basic system performance requirement. It would be used in conjunction with another architecture capable of observing 25 kHz channels at a 100 Hz rate.

The above set of architectures covers a range of approximately 200:1 in observation bandwidth. In all cases, a sampling frequency (fs) of approximately three times the observation bandwidth, or 1.5 times the Nyquist rate, is used.

For the IF architectures, the observation bandwidth is centred at 3fs/4. Because of aliasing in the sampling process, the observation bandwidth in the sampled signal can be considered as being centred at fs/4. This technique is used, as opposed to centring the analog signal at fs/4, to allow the local oscillator for the down-conversion to the final IF to be separated further in frequency from the pre-conversion IF signal.

The observation bandwidth extends from 7fs/12 to 11fs/12 and is aliased into fs/12 to 5fs/12. As shown in Figure 3.2, the signal prior to sampling can extend as far as 5fs/12 and 13fs/12 without causing unwanted aliasing into the observation bandwidth. This can be achieved with a final IF filter having a fractional passband width of (4/12)/(3/4) = 44% and a width at the stopband edges of (8/12)/(3/4) = 89%.

3.5.1 RF Architecture

The RF architecture is conceptually very simple, consisting only of a bandpass filter and an amplifier prior to A/D conversion.

The bandpass filter limits the incoming signal to the range of interest, 30 to 88 MHz. To allow a sampling rate of 3 * 88 = 264 MHz, the filter must provide sufficient attenuation above 264/2 = 132 MHz to limit aliasing to an acceptable level.

Note: the anti-aliasing filter stopband is normally required to begin by fs/2. This allows the signal to be reconstructed correctly. However, in this case we are interested only in the portion of the signal extending up to 88 MHz (fs/3). As shown in Figure 3.3, signal components between fs/3 and 2fs/3 alias into the range fs-fs/3 to fs-2fs/3, which is again fs/3 to 2fs/3, and hence do not affect measurements in the range of interest. This allows a larger transition region for the anti-aliasing filter, or alternatively a lower sampling rate than would normally be required. For example, if the stopband begins at 1.5 * 88 = 132 MHz, a sampling rate of 88 + 132 = 220 MHz is sufficient (see Figure 3.4). In practice, we would like the filter to cut off as sharply as possible, to reject out-of-band interference.

3.5.2 Wide-IF Architecture

The Wide-IF architecture employs a sampling rate of 20 MHz and hence an observation bandwidth of 6.67 MHz and an IF centre frequency of 15 MHz.

The 58 MHz range can be covered in 9 bands. With an observation time of 320 μs, each channel can be observed at a rate of 347 Hz.

3.5.3 Mid-IF Architecture

As derived in section 3.1.1, the minimum observation bandwidth for a frequency resolution of 25/8 kHz and a channel observation rate of 100 Hz is 1.87 MHz.

At 3 times the observation bandwidth, a sampling frequency of 5.61 MHz is required, corresponding to an FFT size of 1795. This can be rounded to the next higher power of two (2048) by using a sampling frequency of 6.4 MHz. The corresponding observation bandwidth is 6.4/3 = 2.133 MHz, and the final IF centre frequency 6.4*3/4 = 4.8 MHz.

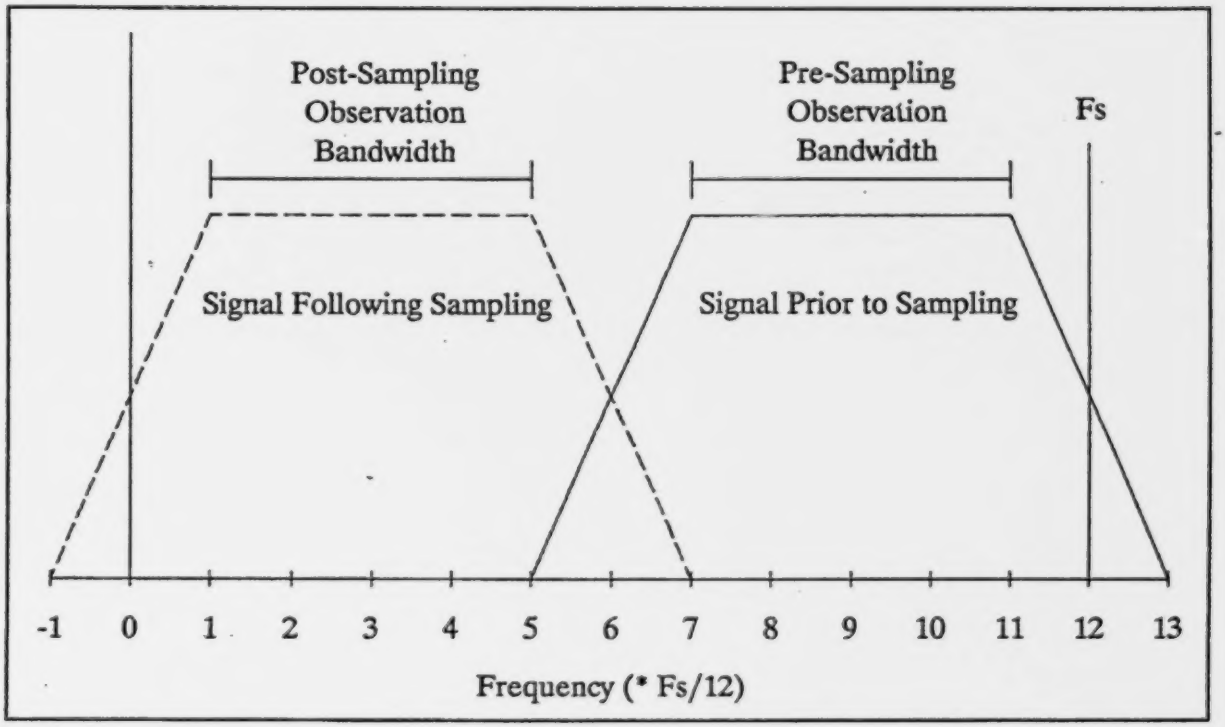


Figure 3.2 IF Architecture Sampling Frequency Plan

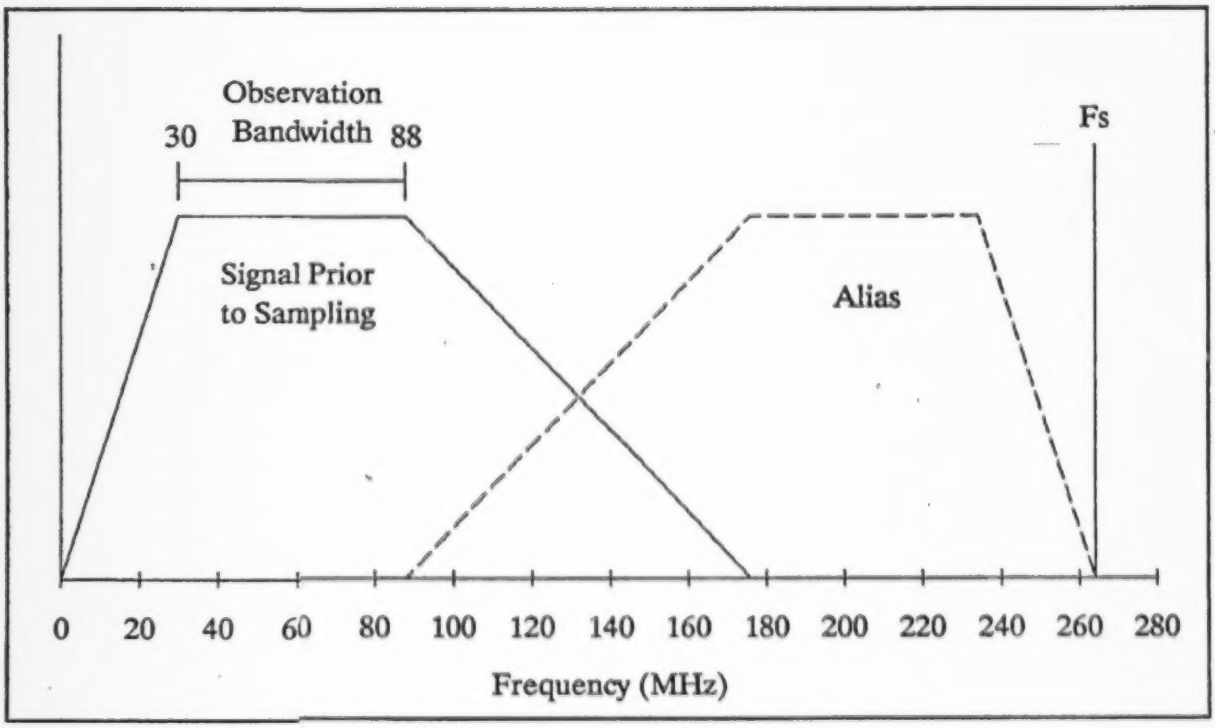


Figure 3.3 RF Architecture Sampling Frequency Plan (Fs = 264 MHz)

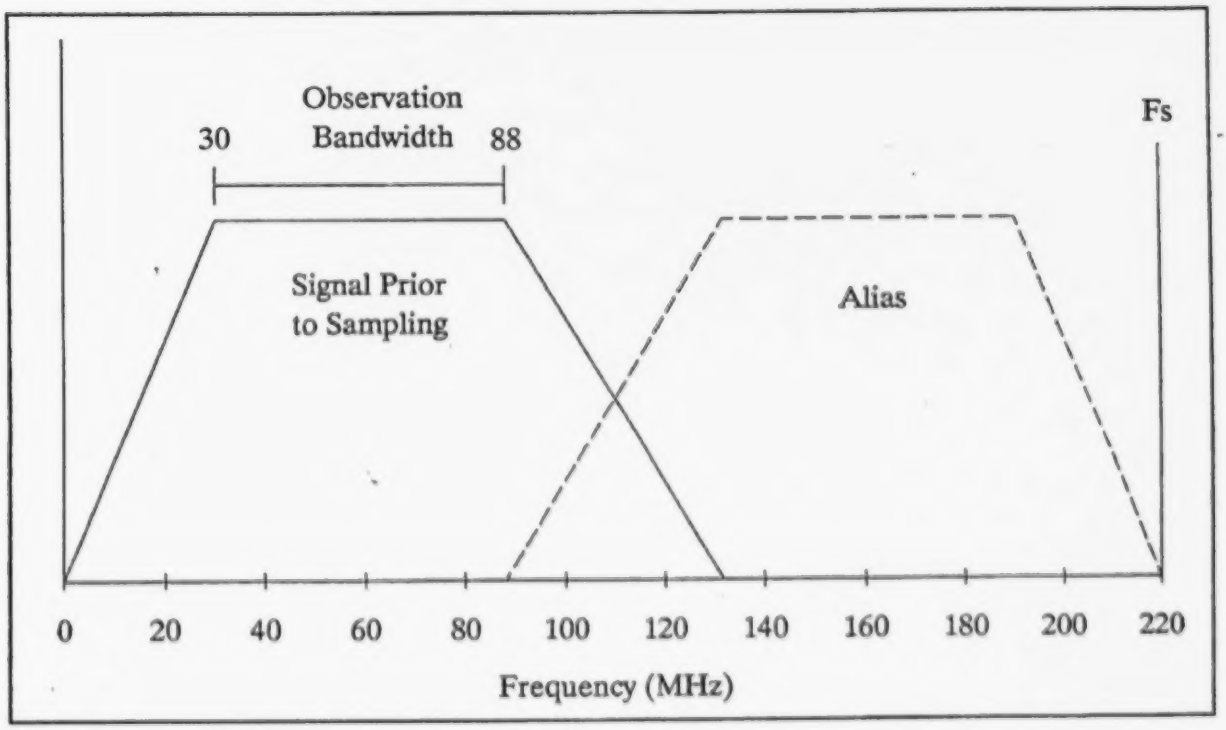


Figure 3.4 RF Architecture Sampling Frequency Plan (Fs = 220 MHz)

For simplicity, we can assume a slightly smaller observation bandwidth of 2 MHz, which allows the 58 MHz range to be covered in 29 bands. For an observation rate of 100 Hz, the total time available for each band is then 345 μs. This allows 25 μs for synthesizer switching and other overhead.

3.5.4 Narrow-IF Architecture

For a maximum FFT size of 2^{16} or 64k, a sampling rate of 65536*100/8 = 819.2 kHz would be required for a bin size of 100/8 = 12.5 Hz. The corresponding observation bandwidth would be approximately 273 kHz, and the final IF centre frequency 614.4 kHz.

The 58 MHz range would be covered in 213 bands. With an observation time of 1/12.5 = 80 ms, each channel could be observed once every 17 seconds. However, the Narrow-IF capability would normally be used to observe only a small portion of the overall coverage range.

4.0 ANALOG PROCESSING

4.1 Performance Requirements

The critical performance parameters for the analog processing components are noise figure and third-order intercept point, which jointly determine the receiver dynamic range. Normally, the lowest noise figure is required for the input amplifier, as it operates at the lowest signal level, and the highest intercept point is required for the output amplifier, as it operates at the highest signal level.

In this application, a noise figure of approximately 10 dB and a spurious-free dynamic range of approximately 100 dB in a 25 kHz bandwidth are desired. For the third-order intermodulation products to be 100 dB below the level of the desired signal, the device in question must be operating 50 dB below its third-order intercept point.

The absolute output power level required is determined by the sensitivity of the A/D converter, with ±1V full-scale being a typical value. If the converter is driven at the standard 50Ω impedance level, the corresponding power for a full-scale sine wave is +10 dBm. This implies a third-order intercept point of +54 dBm for an intermodulation ratio of 100 dB, with two input tones at -6 dB relative to full scale. The maximum output power of an amplifier with a third-order intercept point of +54 dBm would typically be approximately +40 dBm, or 10 watts.

The power required can be reduced by driving the A/D converter at a higher impedance level. This is probably not feasible at the highest sampling rates (e.g., for direct RF digitization), where the A/D input capacitance becomes significant. However, A/D converters suitable for the IF architectures have typical input impedances of at least 1 kΩ, and can conveniently be driven at a 600Ω level.

By using a step-up transformer, the required voltage drive level for the A/D converter can be achieved with a smaller voltage swing, and hence a lower output power, from the final amplifier (assumed to be operating at 50Ω). For example, RF transformers are available with intermodulation ratios in excess of 100 dB which perform a 50Ω to 600Ω conversion. This provides a voltage step-up factor of $\sqrt{12}$, and hence reduces the power required from the amplifier by a factor of 12, or approximately 11 dB. The required third-order intercept point then becomes +43 dBm, corresponding to a maximum output power of somewhat less than 1 watt.

For the case of RF digitization, the amplifier power required may be reduced by other limitations on the dynamic range (e.g., A/D resolution). For example, if the maximum achievable dynamic range is 80 dB, the amplifier third-order intercept point required is +44 dBm and the corresponding maximum output power would be on the order of 1 watt.

Table 4.1 lists the principal performance parameters of a variety of RF amplifiers from several major manufacturers. Spurious-free dynamic range values exceeding 100 dB can be achieved at frequencies of up to 500 MHz. The highest available third-order intercept point is +50 dBm.

No	-174	dBm/Hz							
BW	44	dBHz							
Mfr	Model	Min Freq (MHz)	Max Freq (MHz)	Gain (dB)	NF (dB)	1 dB (dBm)	IP3o (dBm)	IP3i (dBm)	DRs (dB)
ANZAC	AM-109	0.5	60	10.0	4.6	31.0	50.0	40.0	110.3
	AM-124	0.5	100	16.0	3.8	-2.0	12.0	-4.0	81.5
	AM-110	0.5	100	30.0	4.5	23.0	40.0	10.0	90.3
	AM-107	1	100	10.0	1.4	1.0	15.0	5.0	89.1
	AM-162	10	100	15.5	1.3	15.0	32.0	16.5	96.8
	AM-113	10	100	30.0	1.5	18.0	33.0	3.0	87.7
	AM-132	5	200	10.0	4.5	29.0	49.0	39.0	109.7
	AM-134	5	200	15.0	4.8	28.0	47.0	32.0	104.8
	AM-136	5	200	20.0	4.8	29.0	49.0	29.0	102.8
	AM-138	5	200	25.0	5.3	29.0	48.0	23.0	98.5
	AM-140	5	200	29.0	5.4	28.0	47.0	18.0	95.1
	AM-117	10	200	8.0	1.3	11.0	30.0	22.0	100.5
	AM-112	10	200	16.0	2.0	9.0	24.0	8.0	90.7
	AM-119	30	250	8.2	2.3	23.0	40.0	31.8	106.3
	AM-102	5	300	10.0	5.0	17.0	33.0	23.0	98.7
	AM-105	5	300	19.0	5.0	17.0	33.0	14.0	92.7
	AM-108	5	300	28.0	5.0	17.0	33.0	5.0	86.7
	AM-181	10	400	8.5	1.5	12.0	30.0	21.5	100.0
	AM-210	5	500	15.3	1.8	6.5	20.0	4.8	88.6
	AM-143	5	500	16.0	1.9	6.0	22.0	6.0	89.4
	AM-103	5	500	10.0	2.7	11.0	25.0	15.0	94.9
	AM-101	5	500	10.0	3.5	22.0	42.0	32.0	105.7
	AM-123	5	500	10.0	3.5	22.0	42.0	32.0	105.7
	AM-131	5	500	10.0	3.5	22.0	42.0	32.0	105.7
	AM-151	5	500	12.0	5.0	21.0	38.0	26.0	100.7
	AM-147	5	500	17.0	3.5	21.0	35.0	18.0	96.3
	AM-148	5	500	14.0	3.5	3.0	16.0	2.0	85.7
	AM-171	5	500	15.0	2.4	-0.5	12.0	-3.0	83.1
	AM-149	5	500	15.0	5.0	16.0	30.0	15.0	93.3
	AM-156	10	500	12.5	2.0	3.5	18.0	5.5	89.0
	AM-146	10	500	21.0	4.0	24.0	38.0	17.0	95.3
	AM-157	20	500	12.5	5.5	24.0	42.0	29.5	102.7
	AM-212	100	600	8.0	1.5	2.0	20.0	12.0	93.7
	AM-191	100	600	23.5	2.5	23.0	32.0	8.5	90.7
	AM-160	100	600	28.0	1.6	19.0	30.0	2.0	86.9

Table 4.1 RF Amplifier Performance

Mfr	Model	Min Freq (MHz)	Max Freq (MHz)	Gain (dB)	NF (dB)	1 dB (dBm)	IP3o (dBm)	IP3i (dBm)	DRs (dB)
AVANTEK	UTO-514	30	200	15	2	-3	7	-8.0	80.0
	UTO-210	10	200	8	2	11	29	21.0	99.3
	UTO-221	10	200	27	2.5	13.5	27	0.0	85.0
	UTO-211	10	200	7.5	2.7	17	28	20.5	98.5
	UTO-222	20	200	28	3.5	19	32	4.0	87.0
	UTO-250	5	200	30	4	-3	9	-21.0	70.0
	UTO-443	10	400	12.5	4.5	4.5	19	6.5	88.0
	UTO-440	10	400	12.5	4.5	8	23	10.5	90.7
	UTO-441	20	400	13.5	4.5	15	32	18.5	96.0
	UTO-444	10	400	12.5	5	8	22	9.5	89.7
	UTO-421	5	400	27	5.5	6	18	-9.0	77.0
	UTO-410	5	400	15	3	-2	8	-7.0	80.0
	UTO-416	5	400	14	5.5	10	23	9.0	89.0
	UTO-442	10	400	13	5.5	20	33	20.0	96.3
	UTO-511	5	500	15	2.5	-2	8	-7.0	80.3
	UTO-517	5	500	22	2.5	5	15	-7.0	80.3
	UTO-543	10	500	10	2.5	6	22	12.0	93.0
	UTO-510	5	500	15	3	-2	8	-7.0	80.0
	UTO-512	5	500	20	3	7	20	0.0	84.7
	UTO-544	10	500	10	3	12	28	18.0	96.7
	UTO-572	50	500	18	3.5	11	24	6.0	88.3
	UTO-501	5	500	14	4	-2	11	-3.0	82.0
	UTO-521	5	500	27	4	8	18	-9.0	78.0
	UTO-502	5	500	14	4	7	21	7.0	88.7
	UTO-571	50	500	14.5	4	10	27	12.5	92.3
	UTO-524	5	500	30	4	14	27	-3.0	82.0
	UTO-516	5	500	14	4.5	10	23	9.0	89.7
	UTO-520	5	500	14	4.5	12	22	8.0	89.0
	UTO-533	5	500	16	5	14	30	14.0	92.7
	UTO-545	10	500	10	5	17	36	26.0	100.7
	UTO-519	5	500	13	5.5	18	33	20.0	96.3
	UTO-509	5	500	13	5.5	20	35	22.0	97.7
	UTO-513	5	500	16	6	14	31	15.0	92.7
	UTO-518	5	500	13	6	23	38	25.0	99.3
	UTO-523	5	500	23	7	12	25	2.0	83.3
	UTO-503	5	500	9	7	13	33	24.0	98.0
	UTO-515	2	500	12	7	14	28	16.0	92.7
	UTO-505	10	500	9	7	18	33	24.0	98.0
	UTO-546	10	500	10	8	23	38	28.0	100.0
	UTO-561	10	500	11	9	26	39	28.0	99.3
	UTO-504	5	500	6	11	17	34	28.0	98.0

Table 4.1 RF Amplifier Performance

Mfr	Model	Min Freq (MHz)	Max Freq (MHz)	Gain (dB)	NF (dB)	1 dB (dBm)	IP3o (dBm)	IP3i (dBm)	DRs (dB)
W-J	A70	10	250	8	1.7	8	23	15.0	95.5
	A70-1	10	250	8	1.8	13	30	22.0	100.1
	A70-2	10	250	8.5	2.2	19	35	26.5	102.9
	A70-3	20	250	8.5	2.8	23.5	38	29.5	104.5
	A81	20	250	25	2.5	17	28	3.0	87.0
	A81-1	20	250	24.5	2	12.5	23	-1.5	84.3
	A82	20	250	22.5	3.3	20	33	10.5	91.5
	A82-1	20	250	17	3.4	15.4	28	11.0	91.7
	A81-2	20	500	22	2.8	15.8	26	4.0	87.5
	A82-3	20	500	15.9	2.8	9.5	19	3.1	86.9

Table 4.1 RF Amplifier Performance

4.2 System Gain

The minimum overall gain required is that which causes a signal at the upper limit of the dynamic range of the analog circuitry to reach full-scale on the A/D converter. If the A/D converter is the limiting element in the overall system dynamic range, additional gain, controlled either manually or automatically, can be beneficial. This allows better use of the dynamic range of the A/D converter in the absence of high-level signals. Note: if the analog circuitry, rather than the A/D, is the limiting factor, additional gain does not improve performance.

We assume that A/D full scale corresponds to +10 dBm for the RF architecture, and to 0 dBm for the IF architectures (using transformer drive). The target noise figure of 10 dB and bandwidth of 25 kHz imply a minimum discernible signal of -120 dBm. For a 100 dB dynamic range, the maximum input signal is -20 dBm, requiring a minimum system gain of 30 dB for the RF architecture and 20 dB for the IF architectures.

4.2.1 AGC

AGC is employed to avoid overloading in the presence of strong input signals. In this report, we are primarily concerned with its effect on receiver instantaneous spurious-free dynamic range, as defined in section 2.3.3.

An AGC system can be modelled as a set of variable attenuators at various points in the signal path, with the attenuator settings controlled by the signal levels at one or more points.

The optimal strategy for controlling a multi-point AGC system can be derived by considering a signal path consisting of a series of processing elements such as amplifiers and mixers, with a variable attenuator preceding each element. Each processing element is assumed to have a well-defined gain, noise figure, and third-order intermodulation intercept point. The goal is to adjust the attenuators in response to the input signal level to maximize the DR_{SI}.

We assume that the attenuators are initially set to zero attenuation, with no signal applied. As the input signal level is increased, some processing element will be the first to generate a discernible spurious product. As the input level is increased further, attenuation should be introduced just ahead of that element, sufficient to maintain the spurious product at the minimum discernible level. This maximizes the output signal-to-noise ratio while avoiding generating any spurious signals above the MDS.

If the output noise is dominated by the internal noise of the element in question or of succeeding stages, the required attenuation will be equal to the increase in input level. This will result in constant output levels for the desired signal, the spurious product, and the noise.

If the noise is dominated by the preceding stages, the required attenuation will be greater than the increase in input level. For example, assume that the input level increases by 1 dB and an equal amount of attenuation is introduced. The output levels of the desired signal and the spurious product will remain constant, but the output noise level will be reduced by 1 dB, making the spurious product now 1 dB above the new MDS level. Since third-order products change by 3 dB for a 1 dB change in signal level, introducing an additional 0.5 dB of attenuation will reduce the desired signal and the noise by 0.5 dB, but the spurious product by 1.5 dB. The spurious product will now be at the new MDS level.

The attenuation could also have been introduced at an earlier stage; however, this would result in poorer noise performance, as the internal noise of the intervening stages would not have been attenuated. Placing the attenuation as far forward in the signal path as possible takes maximum advantage of the increased input level in reducing the output noise.

As the input level increases still further, a point will be reached at which another stage begins to generate discernible spurious products. Note that this stage must be earlier in the signal path, as the output level from the stage considered first has at most remained constant, and may even have decreased.

The attenuator first adjusted is now left fixed, and that preceding the earlier stage is adjusted as previously described.

This process is repeated as the input level increases, with the point of adjustment moving successively back in the signal path. This continues until the first stage begins to generate discernible spurious products. Subsequent adjustment is then made with the attenuator at the receiver input.

Note: since the spurious products generated by multiple stages are cumulative, the spurious level due to a single stage must actually be kept somewhat below the MDS. The margin required depends on the number of stages that will be contributing significant spurious levels.

4.3 Baseline Front-End Design

This section presents initial designs for the analog front-end processing of the selected architectures.

4.3.1 Frequency Plan

For any frequency-conversion receiver, and particularly for one where a wide spurious-free dynamic range is required, the frequency plan (i.e., the LO and IF frequencies) must be chosen carefully to avoid introducing spurious mixing products into the output.

Any mixing operation theoretically generates output products at the sum and difference of all combinations of harmonics of the input and LO frequencies (i.e., at $|n*f_{IN} \pm m*f_{LO}|$). Hence, there will always be spurious products which fall within the output IF bandwidth, for some combination of harmonics.

The levels of the mixing products normally fall off rapidly with increasing harmonic order, and it is therefore desirable to maximize the minimum order for which spurious products fall within the IF bandwidth. In practice, it is normally sufficient to avoid products of up to the third harmonic of the input frequency and approximately the tenth harmonic of the LO frequency.

To facilitate the choice of frequency plan, a spreadsheet model has been implemented which identifies the spurious products generated from specified input, LO, and IF frequency ranges. With the appropriate input parameters, the model is applicable to all types of frequency conversions, including sum or difference up- or down-conversion, with fixed or variable LO frequency and with wide- or narrowband IF output.

This model is used below to select appropriate frequency plans for the IF architectures.

4.3.1.1 RF Architecture

Since the entire RF band is digitized directly, no frequency conversion is required.

4.3.1.2 Wide-IF Architecture

The Wide-IF architecture employs a final IF of 15 MHz, with an observation bandwidth of 6.67 MHz. Double conversion is required, as single conversion would require the LO frequency to be within the coverage band, which would cause unwanted image responses.

Because the coverage bandwidth exceeds one octave, spurious responses will exist due to the second harmonic of the input signal. The output frequency resulting from the second harmonic of a signal in the range 30 to 44 MHz is the same as the response to the fundamental of a signal in the range 60 to 88 MHz.

This can be avoided entirely only by pre-filtering the input into separate bands of less than an octave each. However, the spurious products due to the second harmonic of the input signal are typically low in level, and hence may be tolerable.

As shown in Table 4.2, using a first IF of 275 MHz with an upper-side LO results in no spurious products below the fourth-order input harmonic, except for the unavoidable second-harmonic response. The LO frequency ranges from from 308.3 MHz to 359.7 MHz, depending on the portion of the coverage band being observed.

Wide-IF Architecture 1st Conversion - 275 MHz IF, Upper-side LO						
	Min	Max				
RF	30.0	88.0				
LO	308.3	359.7				
IF	271.7	278.3				
RF # (n)	LO # (m)	mLO + nRF			mLO - nRF	
		Min	Max		Min	Max
0	0	0.0	0.0		0.0	0.0
0	1	308.3	359.7		308.3	359.7
0	2	616.6	719.4		616.6	719.4
0	3	924.9	1079.1		924.9	1079.1
0	4	1233.2	1438.8		1233.2	1438.8
0	5	1541.5	1798.5		1541.5	1798.5
0	6	1849.8	2158.2		1849.8	2158.2
0	7	2158.1	2517.9		2158.1	2517.9
0	8	2466.4	2877.6		2466.4	2877.6
0	9	2774.7	3237.3		2774.7	3237.3
0	10	3083.0	3597.0		3083.0	3597.0
1	0	30.0	88.0		-88.0	-30.0
1	1	338.3	447.7		220.3	329.7 *
1	2	646.6	807.4		528.6	689.4
1	3	954.9	1167.1		836.9	1049.1
1	4	1263.2	1526.8		1145.2	1408.8
1	5	1571.5	1886.5		1453.5	1768.5
1	6	1879.8	2246.2		1761.8	2128.2
1	7	2188.1	2605.9		2070.1	2487.9
1	8	2496.4	2965.6		2378.4	2847.6
1	9	2804.7	3325.3		2686.7	3207.3
1	10	3113.0	3685.0		2995.0	3567.0
2	0	60.0	176.0		-176.0	-60.0
2	1	368.3	535.7		132.3	299.7 *
2	2	676.6	895.4		440.6	659.4
2	3	984.9	1255.1		748.9	1019.1
2	4	1293.2	1614.8		1057.2	1378.8
2	5	1601.5	1974.5		1365.5	1738.5
2	6	1909.8	2334.2		1673.8	2098.2
2	7	2218.1	2693.9		1982.1	2457.9
2	8	2526.4	3053.6		2290.4	2817.6
2	9	2834.7	3413.3		2598.7	3177.3
2	10	3143.0	3773.0		2907.0	3537.0

Table 4.2 Frequency Conversion Products

Wide-IF Architecture 1st Conversion - 275 MHz IF, Upper-side LO							
3	0	90.0	264.0		-264.0	-90.0	
3	1	398.3	623.7		44.3	269.7	
3	2	706.6	983.4		352.6	629.4	
3	3	1014.9	1343.1		660.9	989.1	
3	4	1323.2	1702.8		969.2	1348.8	
3	5	1631.5	2062.5		1277.5	1708.5	
3	6	1939.8	2422.2		1585.8	2068.2	
3	7	2248.1	2781.9		1894.1	2427.9	
3	8	2556.4	3141.6		2202.4	2787.6	
3	9	2864.7	3501.3		2510.7	3147.3	
3	10	3173.0	3861.0		2819.0	3507.0	
4	0	120.0	352.0	*	-352.0	-120.0	*
4	1	428.3	711.7		-43.7	239.7	
4	2	736.6	1071.4		264.6	599.4	*
4	3	1044.9	1431.1		572.9	959.1	
4	4	1353.2	1790.8		881.2	1318.8	
4	5	1661.5	2150.5		1189.5	1678.5	
4	6	1969.8	2510.2		1497.8	2038.2	
4	7	2278.1	2869.9		1806.1	2397.9	
4	8	2586.4	3229.6		2114.4	2757.6	
4	9	2894.7	3589.3		2422.7	3117.3	
4	10	3203.0	3949.0		2731.0	3477.0	
5	0	150.0	440.0	*	-440.0	-150.0	*
5	1	458.3	799.7		-131.7	209.7	
5	2	766.6	1159.4		176.6	569.4	*
5	3	1074.9	1519.1		484.9	929.1	
5	4	1383.2	1878.8		793.2	1288.8	
5	5	1691.5	2238.5		1101.5	1648.5	
5	6	1999.8	2598.2		1409.8	2008.2	
5	7	2308.1	2957.9		1718.1	2367.9	
5	8	2616.4	3317.6		2026.4	2727.6	
5	9	2924.7	3677.3		2334.7	3087.3	
5	10	3233.0	4037.0		2643.0	3447.0	

Table 4.2 Frequency Conversion Products

If the lower-side rather than the upper-side LO were used, an IF frequency of approximately 450 MHz would be required to provide comparable performance.

The use of the upper-side LO results in frequency inversion of the signal spectrum. This can be taken into account in subsequent processing.

The second conversion is performed with a fixed LO frequency of 290 MHz. As shown in Table 4.3, no spurious products are generated.

4.3.1.3 Mid-IF Architecture

The Mid-IF architecture employs a final IF of 4.8 MHz, with an observation bandwidth of 2.0 MHz. As for the Wide-IF architecture, at least double conversion is required.

The same first IF is used as for the Wide-IF architecture (275 MHz). This can be converted to the final IF using a second LO of 279.8 MHz.

To prevent the 2LO-2RF product from falling into the observation band (3.8 to 5.8 MHz), the upper edge of the pre-conversion bandwidth must be at least 5.8/2 = 2.9 MHz below the LO frequency, and hence not more than 4.8 - 2.9 = 1.9 MHz above the band centre. Assuming the pre-conversion filter to be symmetrical, this implies a fractional bandwidth of 2*1.9/275 = 1.4% at the stopband edges. Simultaneously, the passband must cover 2.0 MHz or 0.73% . Such selectivity is difficult to obtain.

Triple conversion can be used to relax the filtering requirements. For example, a second IF of 35 MHz can be used. For the final conversion (from 35 MHz to 4.8 MHz), the required fractional bandwidth at the stopband edges is then 2*1.9/35 = 10.9%, and the passband bandwidth is 2.0/35 = 5.7%. These values are easily achieved. The stopband edge is offset from the centre frequency by 1.9/2.0 = 0.95 times the passband bandwidth. Approximately 40 dB of attenuation can be obtained at this offset, using an 8-section tubular filter. As the 2LO-2RF product is typically suppressed by at least 65 dB in the mixer itself, this should prevent any detectible spurious products.

As an alternative to triple conversion, a second IF of 7fs/4 = 11.2 MHz can be used, with the observation bandwidth covering 10.2 to 12.2 MHz. In this case, the pre-conversion bandwidth at the stopband edges must be limited to 2*(11.2-12.2/2) = 10.2 MHz, or 3.7%, with a passband bandwidth of at least 0.73%. These values are feasible. Aliasing in the sampling process results in a sampled signal equivalent to what would have be obtained with the original 4.8 MHz IF. Note: to avoid spurious aliasing into the observation bandwidth, the signal must be limited prior to sampling to the range 9.0 to 13.4 MHz, corresponding to a fractional bandwidth of 4.4/11.2 = 39.3%, with a passband of at least 2.0/11.2 = 17.9%.

Wide-IF Architecture 2nd Conversion - 275 MHz 1st IF, Upper-side LO						
	Min	Max				
RF	270.0	280.0				
LO	290.0	290.0				
IF	11.7	18.3				
RF # (n)	LO # (m)	mLO + nRF			mLO - nRF	
		Min	Max		Min	Max
0	0	0.0	0.0		0.0	0.0
0	1	290.0	290.0		290.0	290.0
0	2	580.0	580.0		580.0	580.0
0	3	870.0	870.0		870.0	870.0
0	4	1160.0	1160.0		1160.0	1160.0
0	5	1450.0	1450.0		1450.0	1450.0
0	6	1740.0	1740.0		1740.0	1740.0
0	7	2030.0	2030.0		2030.0	2030.0
0	8	2320.0	2320.0		2320.0	2320.0
0	9	2610.0	2610.0		2610.0	2610.0
0	10	2900.0	2900.0		2900.0	2900.0
1	0	270.0	280.0		-280.0	-270.0
1	1	560.0	570.0		10.0	20.0
1	2	850.0	860.0		300.0	310.0
1	3	1140.0	1150.0		590.0	600.0
1	4	1430.0	1440.0		880.0	890.0
1	5	1720.0	1730.0		1170.0	1180.0
1	6	2010.0	2020.0		1460.0	1470.0
1	7	2300.0	2310.0		1750.0	1760.0
1	8	2590.0	2600.0		2040.0	2050.0
1	9	2880.0	2890.0		2330.0	2340.0
1	10	3170.0	3180.0		2620.0	2630.0
2	0	540.0	560.0		-560.0	-540.0
2	1	830.0	850.0		-270.0	-250.0
2	2	1120.0	1140.0		20.0	40.0
2	3	1410.0	1430.0		310.0	330.0
2	4	1700.0	1720.0		600.0	620.0
2	5	1990.0	2010.0		890.0	910.0
2	6	2280.0	2300.0		1180.0	1200.0
2	7	2570.0	2590.0		1470.0	1490.0
2	8	2860.0	2880.0		1760.0	1780.0
2	9	3150.0	3170.0		2050.0	2070.0
2	10	3440.0	3460.0		2340.0	2360.0

Table 4.3 Frequency Conversion Products

Wide-IF Architecture 2nd Conversion - 275 MHz 1st IF, Upper-side LO						
3	0	810.0	840.0		-840.0	-810.0
3	1	1100.0	1130.0		-550.0	-520.0
3	2	1390.0	1420.0		-260.0	-230.0
3	3	1680.0	1710.0		30.0	60.0
3	4	1970.0	2000.0		320.0	350.0
3	5	2260.0	2290.0		610.0	640.0
3	6	2550.0	2580.0		900.0	930.0
3	7	2840.0	2870.0		1190.0	1220.0
3	8	3130.0	3160.0		1480.0	1510.0
3	9	3420.0	3450.0		1770.0	1800.0
3	10	3710.0	3740.0		2060.0	2090.0
4	0	1080.0	1120.0		-1120.0	-1080.0
4	1	1370.0	1410.0		-830.0	-790.0
4	2	1660.0	1700.0		-540.0	-500.0
4	3	1950.0	1990.0		-250.0	-210.0
4	4	2240.0	2280.0		40.0	80.0
4	5	2530.0	2570.0		330.0	370.0
4	6	2820.0	2860.0		620.0	660.0
4	7	3110.0	3150.0		910.0	950.0
4	8	3400.0	3440.0		1200.0	1240.0
4	9	3690.0	3730.0		1490.0	1530.0
4	10	3980.0	4020.0		1780.0	1820.0
5	0	1350.0	1400.0		-1400.0	-1350.0
5	1	1640.0	1690.0		-1110.0	-1060.0
5	2	1930.0	1980.0		-820.0	-770.0
5	3	2220.0	2270.0		-530.0	-480.0
5	4	2510.0	2560.0		-240.0	-190.0
5	5	2800.0	2850.0		50.0	100.0
5	6	3090.0	3140.0		340.0	390.0
5	7	3380.0	3430.0		630.0	680.0
5	8	3670.0	3720.0		920.0	970.0
5	9	3960.0	4010.0		1210.0	1260.0
5	10	4250.0	4300.0		1500.0	1550.0

Table 4.3 Frequency Conversion Products

The second alternative is preferable for its reduced complexity. A potential disadvantage is that it requires the A/D converter, although still operating at a 6.4 MHz sample rate, to accept an input signal of approximately twice the frequency. This places greater demands on the sample-and-hold and other front-end circuitry of the converter.

As shown in Table 4.4, no spurious products are generated by the proposed frequency conversions.

4.3.1.4 Narrow-IF Architecture

The Narrow-IF architecture employs an observation bandwidth of 273 kHz, with a sampling rate of 819.2 kHz and a nominal IF of 3/4 the sampling rate, or 614.4 kHz. However, this would involve an additional down-conversion stage beyond those required for the Wide- or Mid-IF architectures.

As was described for the for the Mid-IF architecture, aliasing in the sampling process can be used to substitute for the final down-conversion. In this case, the pre-sampling observation bandwidth would be centred at (n+3/4)fs, with n (an integer) chosen to place the observation bandwidth within the passband of the final IF of the Wide- or Mid-IF architecture. For example, assuming that the Mid-IF architecture is used with a passband of 10.2 to 12.2 MHz, n can be chosen as 13, centring the observation bandwidth at 13.75*0.8192 = 11.264 MHz. The signal must be limited prior to sampling a bandwidth of 2fs/3 = 546 kHz, or 4.8%, with a passband of at least fs/3 = 273 kHz, or 2.4%.

This approach is again attractively simple, but makes greater demands on the A/D converter than would the use of the nominal IF of 614.4 kHz.

4.3.2 Performance

Figures 4.5 and 4.6 show the performance achievable by candidate implementations of the front-end designs for the RF and IF architectures, using readily available devices.

The RF architecture has the best performance, with a noise figure of 5.9 dB and a dynamic range of 96.6 dB.

All three IF architectures (Wide, Mid, and Narrow) can be implemented with the same components (except for filter parameters), and have the same analog performance: a noise figure of 9.3 dB and a dynamic range of 93.7 dB. This assumes that bandpass sampling is used as described for the Mid- and Narrow-IF architectures, centring the final IF at 11.2 or 11.264 MHz and making double conversion sufficient.

Mid-IF Architecture 2nd Conversion - 275 MHz 1st IF, Upper-side LO						
	Min	Max	BW		Prev IF	Prev BW
RF	273.105	276.895	1.4%		275.000	3.790
LO	279.800	279.800	0.0%		New IF	New BW
IF	3.800	5.800	41.7%		4.800	2.000
RF # (n)	LO # (m)	mLO + nRF			mLO - nRF	
		Min	Max		Min	Max
0	0	0.000	0.000		0.000	0.000
0	1	279.800	279.800		279.800	279.800
0	2	559.600	559.600		559.600	559.600
0	3	839.400	839.400		839.400	839.400
0	4	1119.200	1119.200		1119.200	1119.200
0	5	1399.000	1399.000		1399.000	1399.000
0	6	1678.800	1678.800		1678.800	1678.800
0	7	1958.600	1958.600		1958.600	1958.600
0	8	2238.400	2238.400		2238.400	2238.400
0	9	2518.200	2518.200		2518.200	2518.200
0	10	2798.000	2798.000		2798.000	2798.000
1	0	273.105	276.895		-276.895	-273.105
1	1	552.905	556.695		2.905	6.695 *
1	2	832.705	836.495		282.705	286.495
1	3	1112.505	1116.295		562.505	566.295
1	4	1392.305	1396.095		842.305	846.095
1	5	1672.105	1675.895		1122.105	1125.895
1	6	1951.905	1955.695		1401.905	1405.695
1	7	2231.705	2235.495		1681.705	1685.495
1	8	2511.505	2515.295		1961.505	1965.295
1	9	2791.305	2795.095		2241.305	2245.095
1	10	3071.105	3074.895		2521.105	2524.895
2	0	546.210	553.790		-553.790	-546.210
2	1	826.010	833.590		-273.990	-266.410
2	2	1105.810	1113.390		5.810	13.390
2	3	1385.610	1393.190		285.610	293.190
2	4	1665.410	1672.990		565.410	572.990
2	5	1945.210	1952.790		845.210	852.790
2	6	2225.010	2232.590		1125.010	1132.590
2	7	2504.810	2512.390		1404.810	1412.390
2	8	2784.610	2792.190		1684.610	1692.190
2	9	3064.410	3071.990		1964.410	1971.990
2	10	3344.210	3351.790		2244.210	2251.790

Table 4.4 (a) Frequency Conversion Products - 4.8 MHz 2nd IF

Mid-IF Architecture 2nd Conversion - 275 MHz 1st IF, Upper-side LO					
RF # (n)	LO # (m)	mLO + nRF		mLO - nRF	
		Min	Max	Min	Max
3	0	819.315	830.685	-830.685	-819.315
3	1	1099.115	1110.485	-550.885	-539.515
3	2	1378.915	1390.285	-271.085	-259.715
3	3	1658.715	1670.085	8.715	20.085
3	4	1938.515	1949.885	288.515	299.885
3	5	2218.315	2229.685	568.315	579.685
3	6	2498.115	2509.485	848.115	859.485
3	7	2777.915	2789.285	1127.915	1139.285
3	8	3057.715	3069.085	1407.715	1419.085
3	9	3337.515	3348.885	1687.515	1698.885
3	10	3617.315	3628.685	1967.315	1978.685
4	0	1092.420	1107.580	-1107.580	-1092.420
4	1	1372.220	1387.380	-827.780	-812.620
4	2	1652.020	1667.180	-547.980	-532.820
4	3	1931.820	1946.980	-268.180	-253.020
4	4	2211.620	2226.780	11.620	26.780
4	5	2491.420	2506.580	291.420	306.580
4	6	2771.220	2786.380	571.220	586.380
4	7	3051.020	3066.180	851.020	866.180
4	8	3330.820	3345.980	1130.820	1145.980
4	9	3610.620	3625.780	1410.620	1425.780
4	10	3890.420	3905.580	1690.420	1705.580
5	0	1365.525	1384.475	-1384.475	-1365.525
5	1	1645.325	1664.275	-1104.675	-1085.725
5	2	1925.125	1944.075	-824.875	-805.925
5	3	2204.925	2223.875	-545.075	-526.125
5	4	2484.725	2503.675	-265.275	-246.325
5	5	2764.525	2783.475	14.525	33.475
5	6	3044.325	3063.275	294.325	313.275
5	7	3324.125	3343.075	574.125	593.075
5	8	3603.925	3622.875	853.925	872.875
5	9	3883.725	3902.675	1133.725	1152.675
5	10	4163.525	4182.475	1413.525	1432.475

Table 4.4 (a) Frequency Conversion Products - 4.8 MHz 2nd IF

Mid-IF Architecture 2nd Conversion - 275 MHz 1st IF, Upper-side LO							
	Min	Max	BW		Prev IF	Prev BW	
RF	270.000	280.000	3.6%		275.000	10.000	
LO	286.200	286.200	0.0%		New IF	New BW	
IF	10.200	12.200	17.9%		11.200	2.000	
RF # (n)	LO # (m)	mLO + nRF			mLO - nRF		
		Min	Max		Min	Max	
0	0	0.000	0.000		0.000	0.000	
0	1	286.200	286.200		286.200	286.200	
0	2	572.400	572.400		572.400	572.400	
0	3	858.600	858.600		858.600	858.600	
0	4	1144.800	1144.800		1144.800	1144.800	
0	5	1431.000	1431.000		1431.000	1431.000	
0	6	1717.200	1717.200		1717.200	1717.200	
0	7	2003.400	2003.400		2003.400	2003.400	
0	8	2289.600	2289.600		2289.600	2289.600	
0	9	2575.800	2575.800		2575.800	2575.800	
0	10	2862.000	2862.000		2862.000	2862.000	
1	0	270.000	280.000		-280.000	-270.000	
1	1	556.200	566.200		6.200	16.200	*
1	2	842.400	852.400		292.400	302.400	
1	3	1128.600	1138.600		578.600	588.600	
1	4	1414.800	1424.800		864.800	874.800	
1	5	1701.000	1711.000		1151.000	1161.000	
1	6	1987.200	1997.200		1437.200	1447.200	
1	7	2273.400	2283.400		1723.400	1733.400	
1	8	2559.600	2569.600		2009.600	2019.600	
1	9	2845.800	2855.800		2295.800	2305.800	
1	10	3132.000	3142.000		2582.000	2592.000	
2	0	540.000	560.000		-560.000	-540.000	
2	1	826.200	846.200		-273.800	-253.800	
2	2	1112.400	1132.400		12.400	32.400	
2	3	1398.600	1418.600		298.600	318.600	
2	4	1684.800	1704.800		584.800	604.800	
2	5	1971.000	1991.000		871.000	891.000	
2	6	2257.200	2277.200		1157.200	1177.200	
2	7	2543.400	2563.400		1443.400	1463.400	
2	8	2829.600	2849.600		1729.600	1749.600	
2	9	3115.800	3135.800		2015.800	2035.800	
2	10	3402.000	3422.000		2302.000	2322.000	

Table 4.4 (b) Frequency Conversion Products - 11.2 MHz 2nd IF

Mid-IF Architecture 2nd Conversion - 275 MHz 1st IF, Upper-side LO					
RF # (n)	LO # (m)	mLO + nRF		mLO - nRF	
		Min	Max	Min	Max
3	0	810.000	840.000	-840.000	-810.000
3	1	1096.200	1126.200	-553.800	-523.800
3	2	1382.400	1412.400	-267.600	-237.600
3	3	1668.600	1698.600	18.600	48.600
3	4	1954.800	1984.800	304.800	334.800
3	5	2241.000	2271.000	591.000	621.000
3	6	2527.200	2557.200	877.200	907.200
3	7	2813.400	2843.400	1163.400	1193.400
3	8	3099.600	3129.600	1449.600	1479.600
3	9	3385.800	3415.800	1735.800	1765.800
3	10	3672.000	3702.000	2022.000	2052.000
4	0	1080.000	1120.000	-1120.000	-1080.000
4	1	1366.200	1406.200	-833.800	-793.800
4	2	1652.400	1692.400	-547.600	-507.600
4	3	1938.600	1978.600	-261.400	-221.400
4	4	2224.800	2264.800	24.800	64.800
4	5	2511.000	2551.000	311.000	351.000
4	6	2797.200	2837.200	597.200	637.200
4	7	3083.400	3123.400	883.400	923.400
4	8	3369.600	3409.600	1169.600	1209.600
4	9	3655.800	3695.800	1455.800	1495.800
4	10	3942.000	3982.000	1742.000	1782.000
5	0	1350.000	1400.000	-1400.000	-1350.000
5	1	1636.200	1686.200	-1113.800	-1063.800
5	2	1922.400	1972.400	-827.600	-777.600
5	3	2208.600	2258.600	-541.400	-491.400
5	4	2494.800	2544.800	-255.200	-205.200
5	5	2781.000	2831.000	31.000	81.000
5	6	3067.200	3117.200	317.200	367.200
5	7	3353.400	3403.400	603.400	653.400
5	8	3639.600	3689.600	889.600	939.600
5	9	3925.800	3975.800	1175.800	1225.800
5	10	4212.000	4262.000	1462.000	1512.000

Table 4.4 (b) Frequency Conversion Products - 11.2 MHz 2nd IF

Stage	Device				Cascade		DRS in
	Model	Gain	NF	IP3o	Gain	NF	25 kHz
		(dB)	(dB)	(dBm)	(dB)	(dB)	(dB)
RF bandpass filter		-2.00	2.00	100.00	-2.00	2.00	150.60
RF amplifier	AM-131	10.00	3.50	42.00	8.00	5.50	105.68
Pad		0.00	0.00	100.00	8.00	5.50	105.68
RF amplifier	AM-136	20.00	4.80	49.00	28.00	5.88	96.62

Table 4.5 RF Architecture Front-End Design

Stage	Device				Cascade		DRS in
	Model	Gain	NF	IP3o	Gain	NF	25 kHz
		(dB)	(dB)	(dBm)	(dB)	(dB)	(dB)
RF bandpass filter		-2.00	2.00	100.00	-2.00	2.00	150.60
RF amplifier	AM-131	10.00	3.50	42.00	8.00	5.50	105.68
Pad		0.00	0.00	100.00	8.00	5.50	105.68
Mixer	W-J M9E	-6.00	6.00	26.00	2.00	6.04	98.38
IF filter (275 MHz)		-2.00	2.00	100.00	0.00	6.42	98.12
IF amplifier	AM-131	10.00	3.50	42.00	10.00	7.50	97.01
Pad		-2.00	2.00	100.00	8.00	7.55	96.98
Mixer	W-J M9E	-6.00	6.00	26.00	2.00	7.90	95.06
IF filter (15/11.2 MHz)		-2.00	2.00	100.00	0.00	8.15	94.89
IF amplifier	AM-136	20.00	4.80	49.00	20.00	9.32	93.73

Table 4.6 IF Architecture Front-End Design

5.0 A/D CONVERSION

5.1 Design Relationships

5.1.1 Quantizing Noise

The fundamental degradation introduced by A/D conversion is quantizing noise, representing the difference between the applied signal level and its quantized digitial value. For an ideal device, the quantizing noise is limited to the range $\pm \frac{1}{2} q$, where q is the quantizing resolution.

The quantizing noise values are normally uniformly distributed in amplitude. For an n-bit A/D, the resulting quantizing noise power is 6.02n + 1.76 dB below the power of a full-scale sine wave. This gives the conventional SNR ratings of 50 dB for 8-bit conversion, 74 dB for 12-bit conversion, etc.

The quantizing noise can often be assumed to be independent from sample to sample, and hence to have a uniform spectral density over the frequency range 0 to $f_s/2$, where f_s is the sampling frequency.

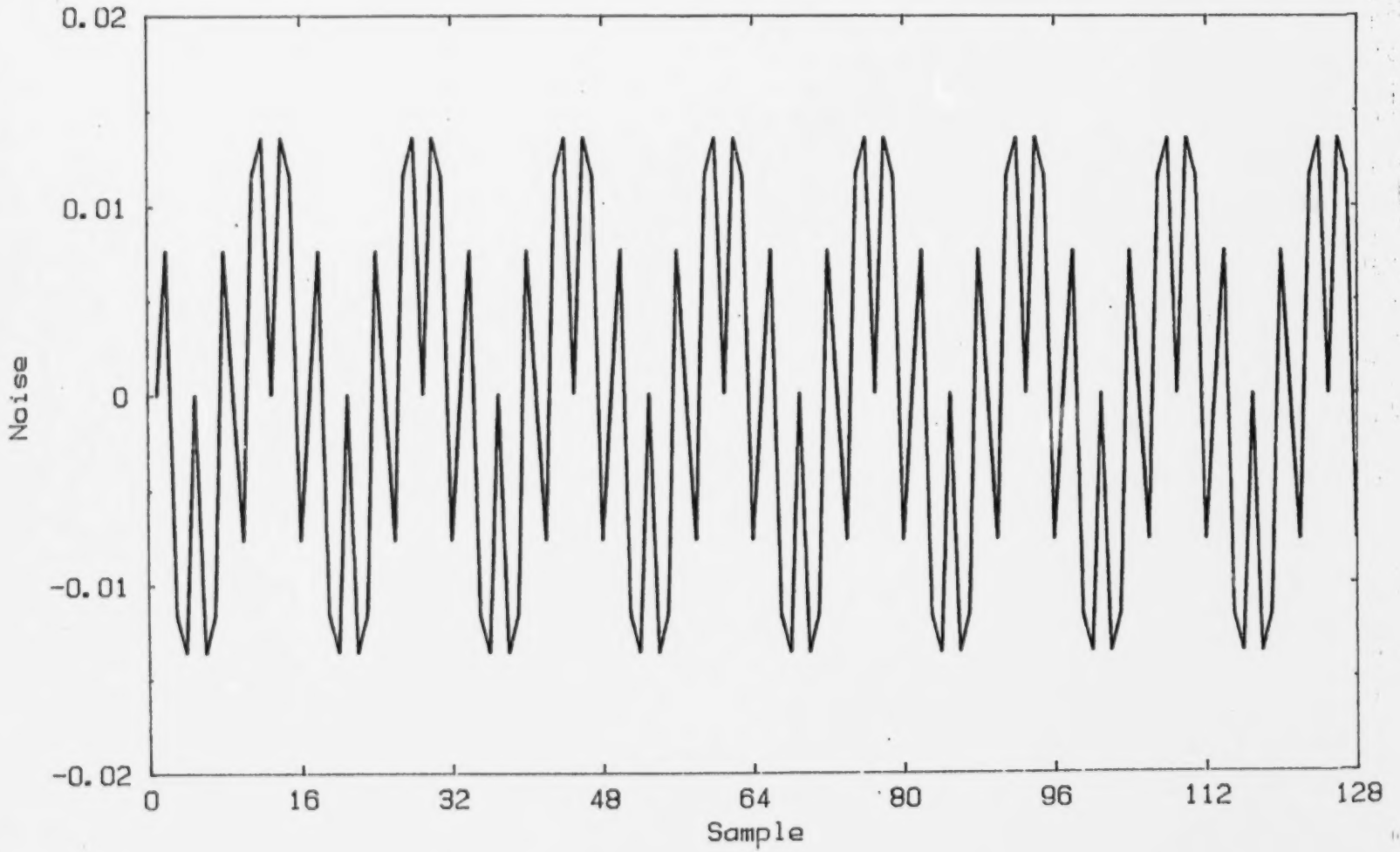
For a surveillance receiver, the parameter of interest is normally the integrated noise power over the detection bandwidth f_d. With uncorrelated quantizing noise, this will be equal to $f_d/(f_s/2)$ times the total quantizing noise power. The SNR in the detection bandwidth can hence be much greater than the overall SNR calculated above.

For example, with 12-bit conversion, 20 MHz sampling, and a 25 kHz detection bandwidth, the resulting SNR is 100.0 dB.

To obtain this SNR improvement, it is necessary that the quantizing noise be uncorrelated. This is normally the case when the signal is such that several quantization levels are traversed between samples. However, in certain cases the quantizing noise can be highly correlated, leading to discrete components in the noise spectrum. This has the same effect as harmonic or intermodulation distortion in generating spurious signals, and hence limiting the dynamic range of the receiver.

Figure 5.1 shows the quantizing noise resulting from 6-bit conversion of a sine wave of amplitude ±1, corresponding to full scale. The quantizing noise is clearly highly correlated, leading to discrete spectral components at harmonics of the signal frequency (see Figure 5.2).

The correlation can be eliminated by adding uncorrelated noise to the input signal. Figure 5.3 shows the effect of adding white Gaussian noise with a standard deviation equal to the quantizing resolution. There is a uniform noise floor, but the discrete components are absent. (Note that the noise floor is about 10 dB below the previous level of the largest harmonics - they have not just been obscured by the noise.)



128
16
64 6-BIT LSB = 0.03125

Figure 5.1 Quantizing Noise

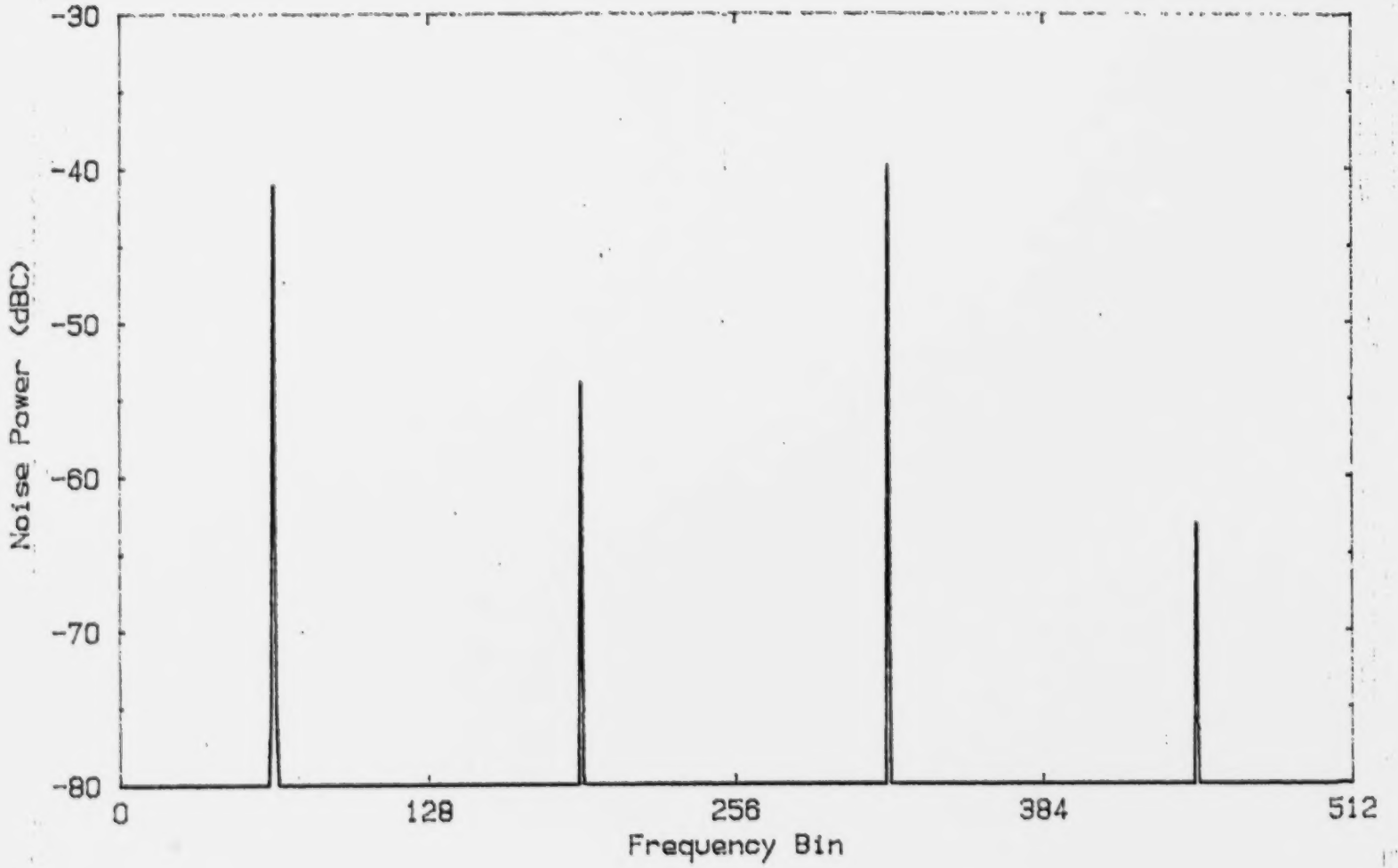
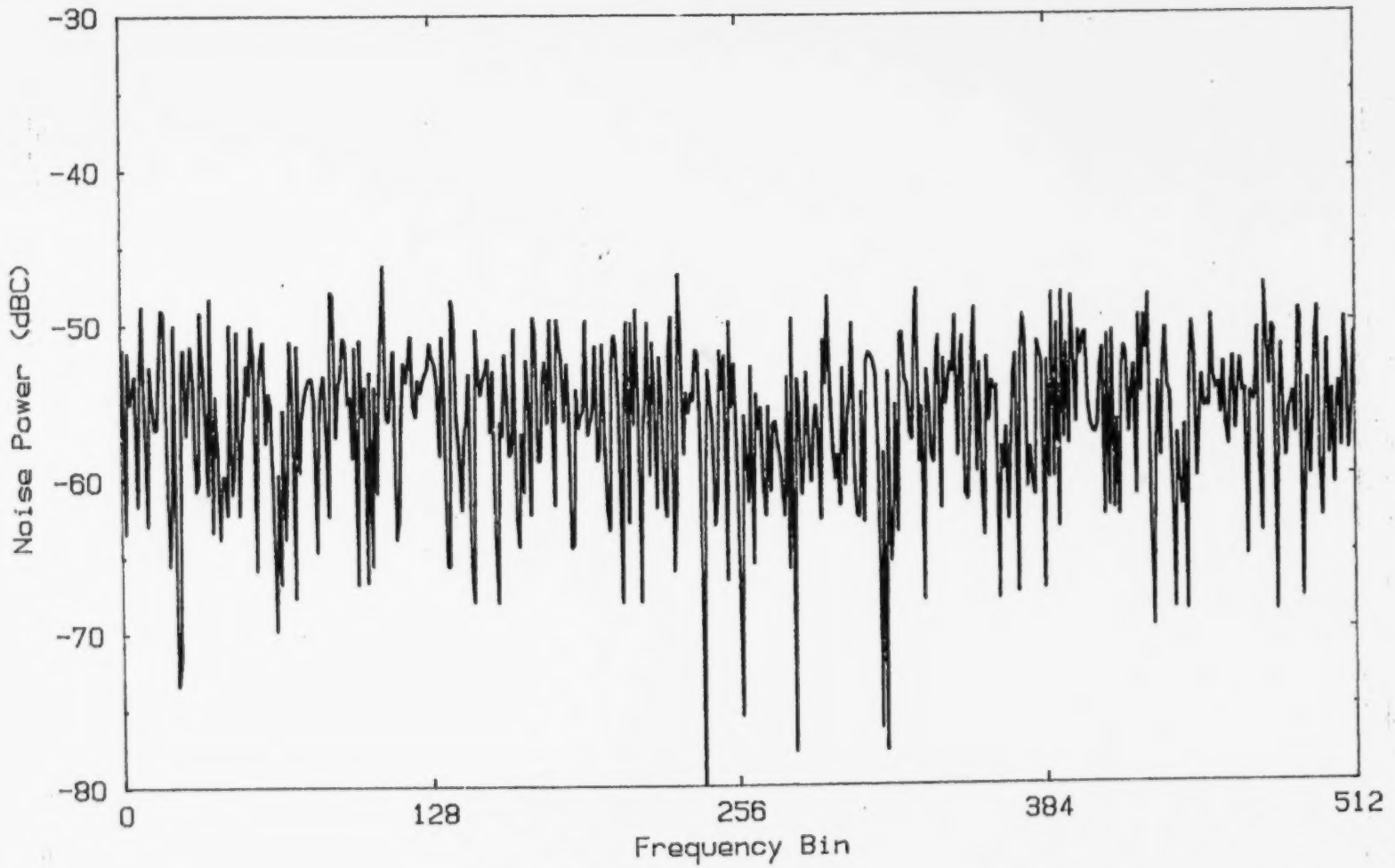


Figure 5.2 Quantizing Noise Power Spectrum

1024
16
64
0
0 NO DITHER



1024
16
64
0.03 GAUSSIAN σ = 1 LSB
0

Figure 5.3 Quantizing Noise Power Spectrum (AWGN = 1 LSB)

Figures 5.4 to 5.6 show the effect of reducing the level of the Gaussian noise. The noise floor drops, and the discrete components begin to re-appear when the standard deviation falls below about 1/4 of the quantizing resolution.

Receiver noise of at least this level would normally be present, and hence would work to decorrelate the quantizing noise. However, if it is desired to maximize the SNR improvement by sampling at a very high rate, the bandwidth of the noise may not be sufficient. In this case, additional noise can be added deliberately. This procedure, known as dithering, has the advantage that the added noise values can potentially be subtracted from the digitized sample values, thus avoiding raising the noise floor.

Figure 5.7 shows the effect of dithering with noise samples uniformly distributed over the range of one quantizing level. The discrete components are absent, but re-appear if the noise level is reduced by half (see Figure 5.8).

Figure 5.9 shows the benefit of subtracting the dither noise values following quantization. Here the dither magnitude was equal to 10 quantizing levels, but the noise floor has not increased.

5.1.2 Aperture Uncertainty

The aperture uncertainty of a sample-and-hold device indicates the variation in the actual time at which the input waveform is sampled, relative to the nominal sampling instant. This variation introduces an error in the sampled value, with the magnitude of the error proportional to the rate of change of the input signal. To achieve the expected SNR from the A/D conversion, the aperture uncertainty must be appropriate for the A/D resolution and the input signal frequency.

As an example, consider n-bit A/D conversion covering the range ±1 V, with a full-scale sine wave input at frequency f. The worst case is at the zero-crossings of the signal, where the rate of change is $2\pi f$ V/s. To limit the error to less than one LSB, the aperture uncertainty must be less than $\frac{1}{2^n \pi f}$.

For 12-bit sampling of a full-scale 10 MHz signal, this requires an aperture uncertainty of less than 8 ps. Commercial sample-and-hold devices are available with aperture uncertainties of approximately 2 ps.

The amplitude of the noise component resulting from aperture uncertainty can be estimated as the product of the rms aperture uncertainty and the rms derivative of the input signal. For a signal normalized to unity power and with uniform spectral density over a bandwidth of W Hz, the total power of the derivative is $\frac{4}{3}\pi^2 W^2$. The noise power is therefore approximately equal to $\frac{4}{3}\pi^2 W^2 \tau^2$, where τ is the rms aperture uncertainty.

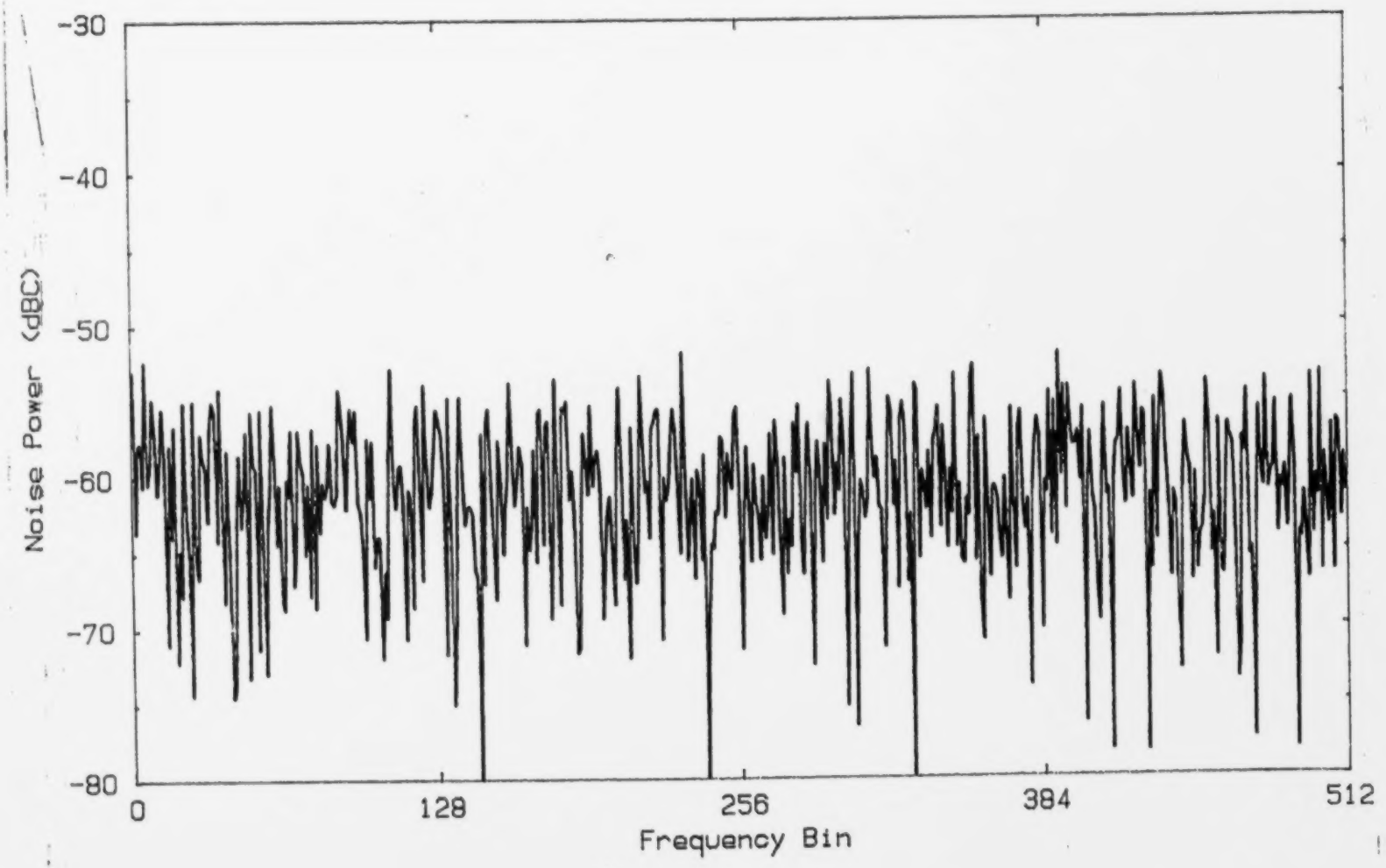


Figure 5.4 Quantizing Noise Power Spectrum (AWGN = 1/2 LSB)

1024
16
64

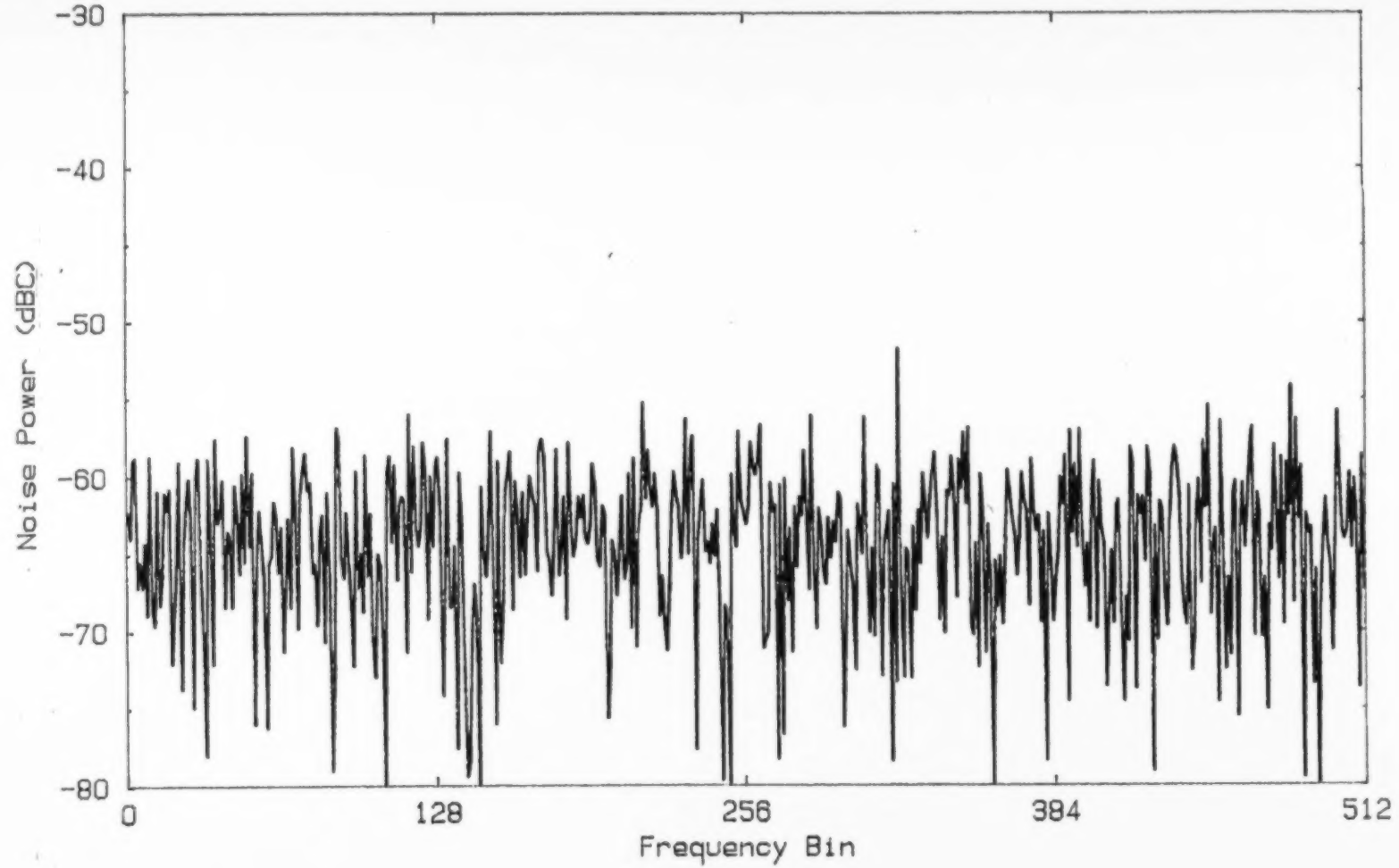


Figure 5.5 Quantizing Noise Power Spectrum (AWGN = 1/4 LSB)

1024
16
64

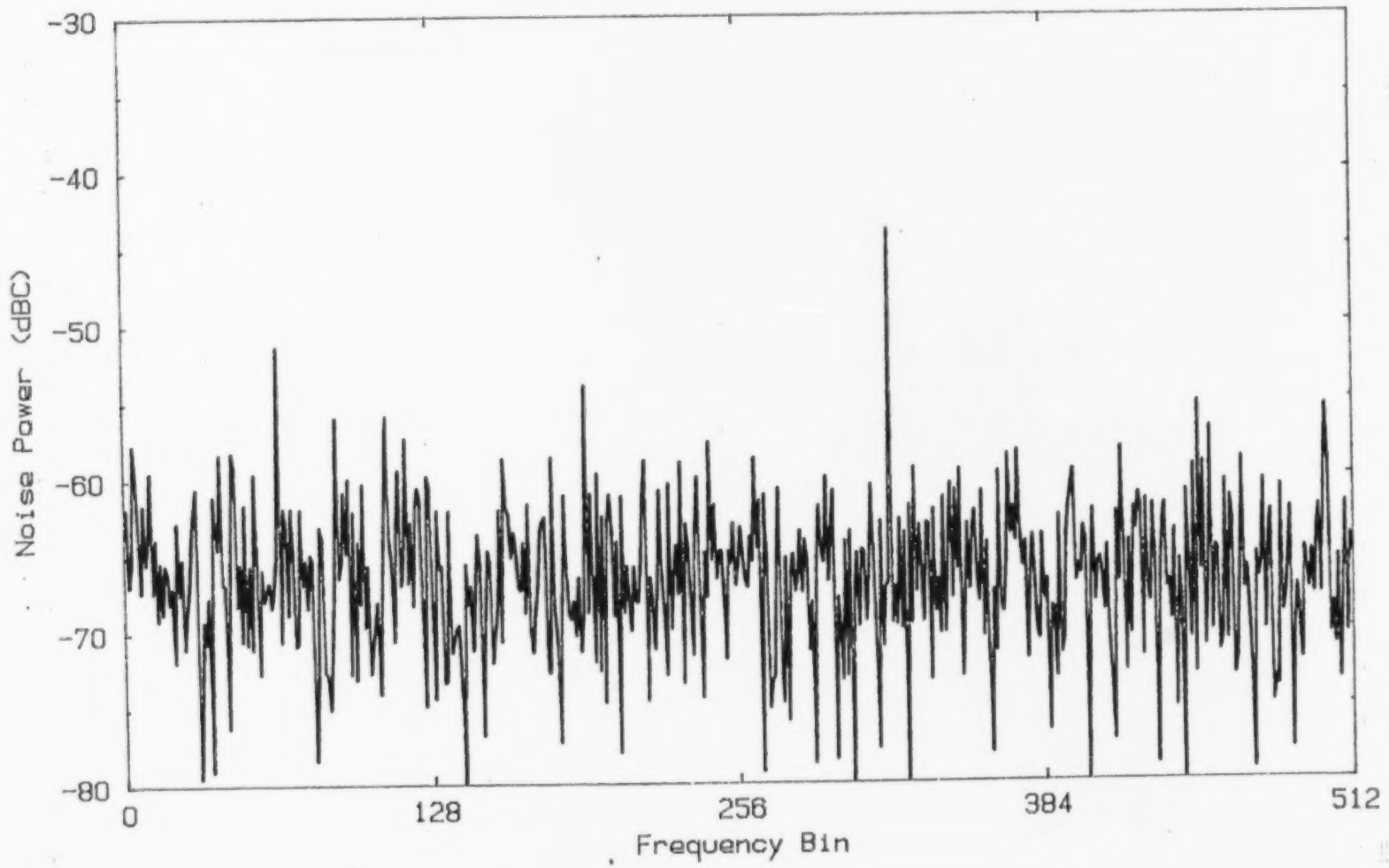


Figure 5.6 Quantizing Noise Power Spectrum (AWGN = 1/8 LSB)

1024
16
64
0.00375 GAUSSIAN $\sigma = \frac{1}{8}$ LSB

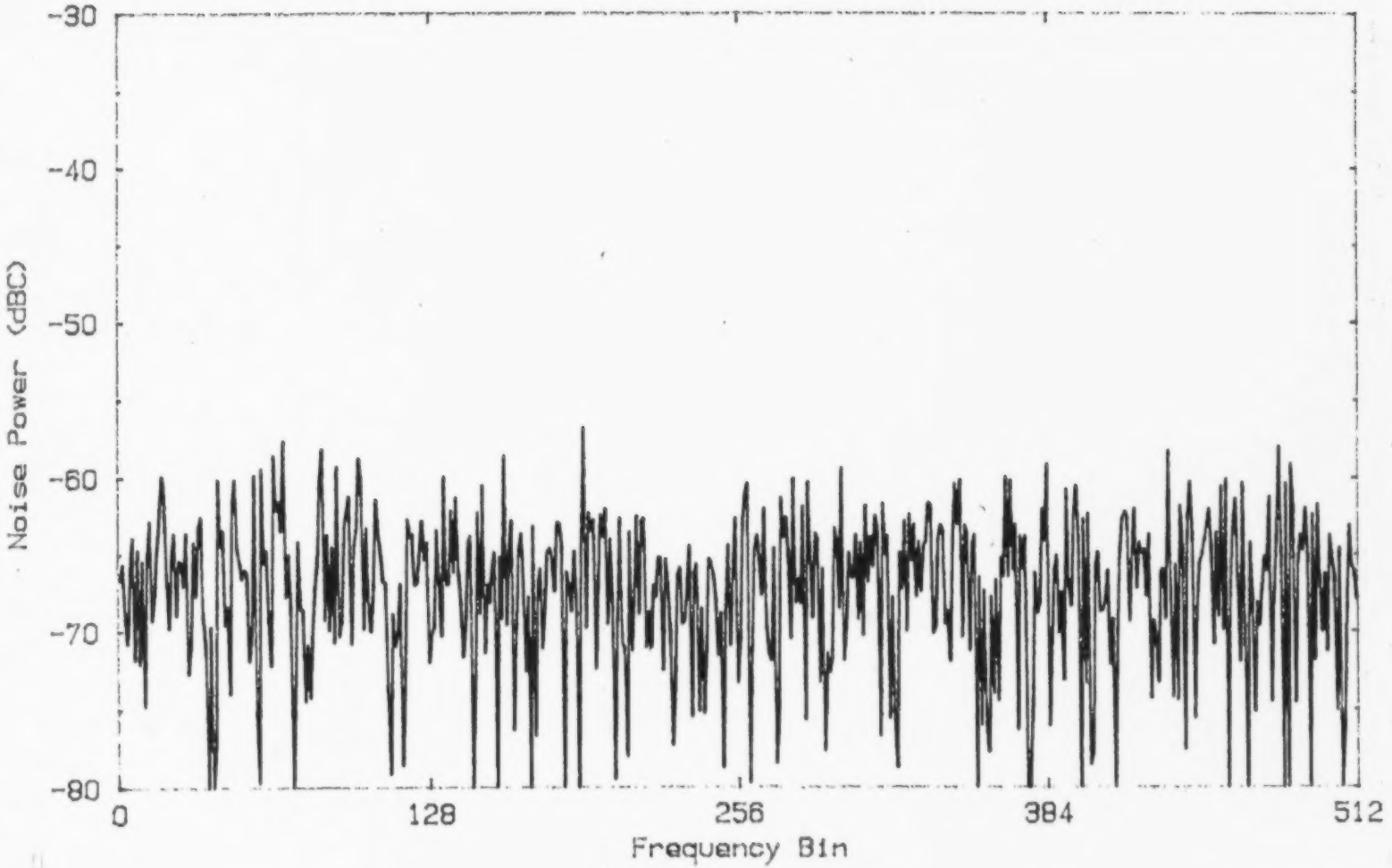


Figure 5.7 Quantizing Noise Power Spectrum (Dither = 1 LSB)

1024
16
64
0
1 DITHER = 1 LSB pk-pk

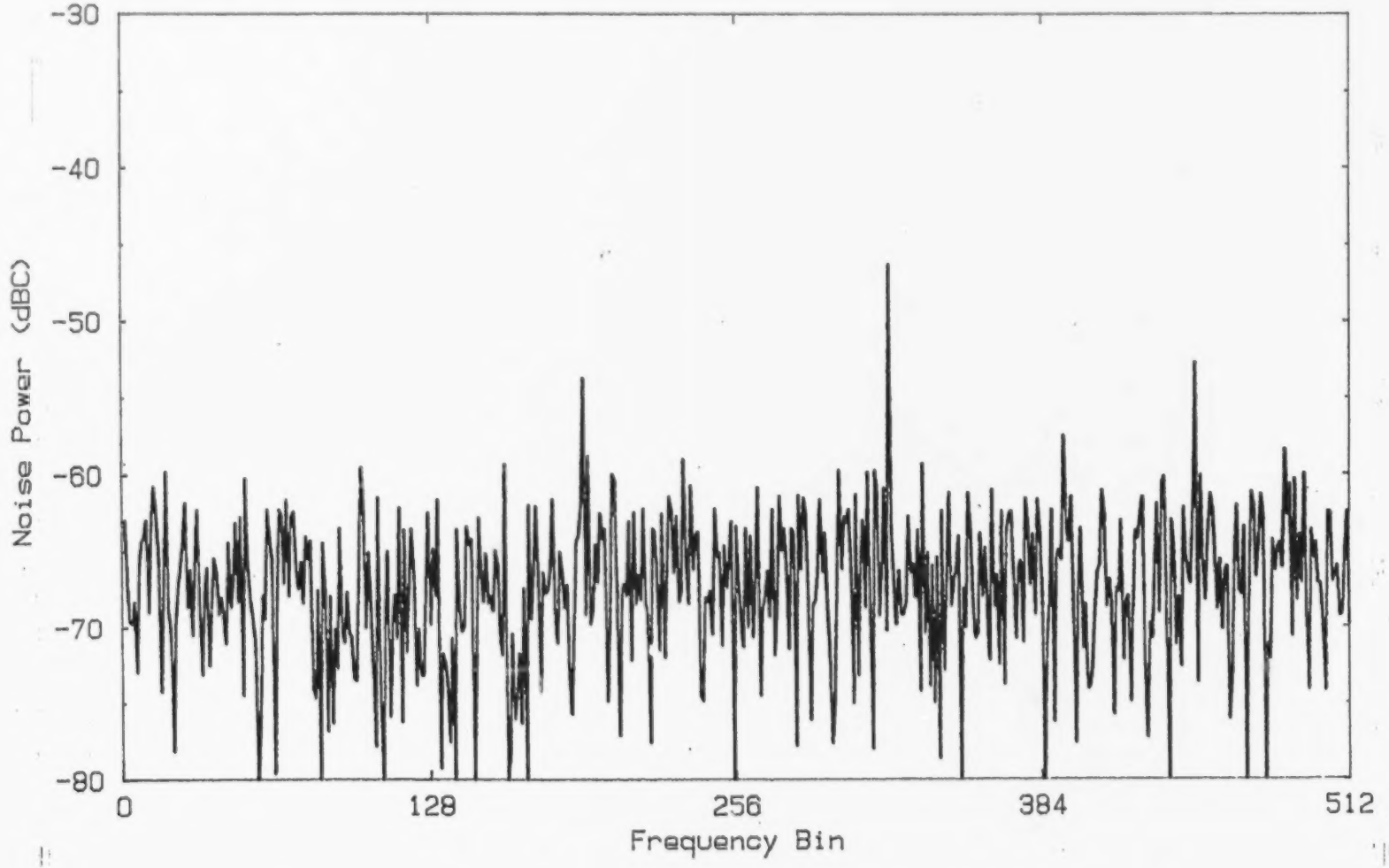


Figure 5.8 Quantizing Noise Power Spectrum (Dither = 1/2 LSB)

1024
16
64
0
0.5 DITHER ½ LSB pk-pk

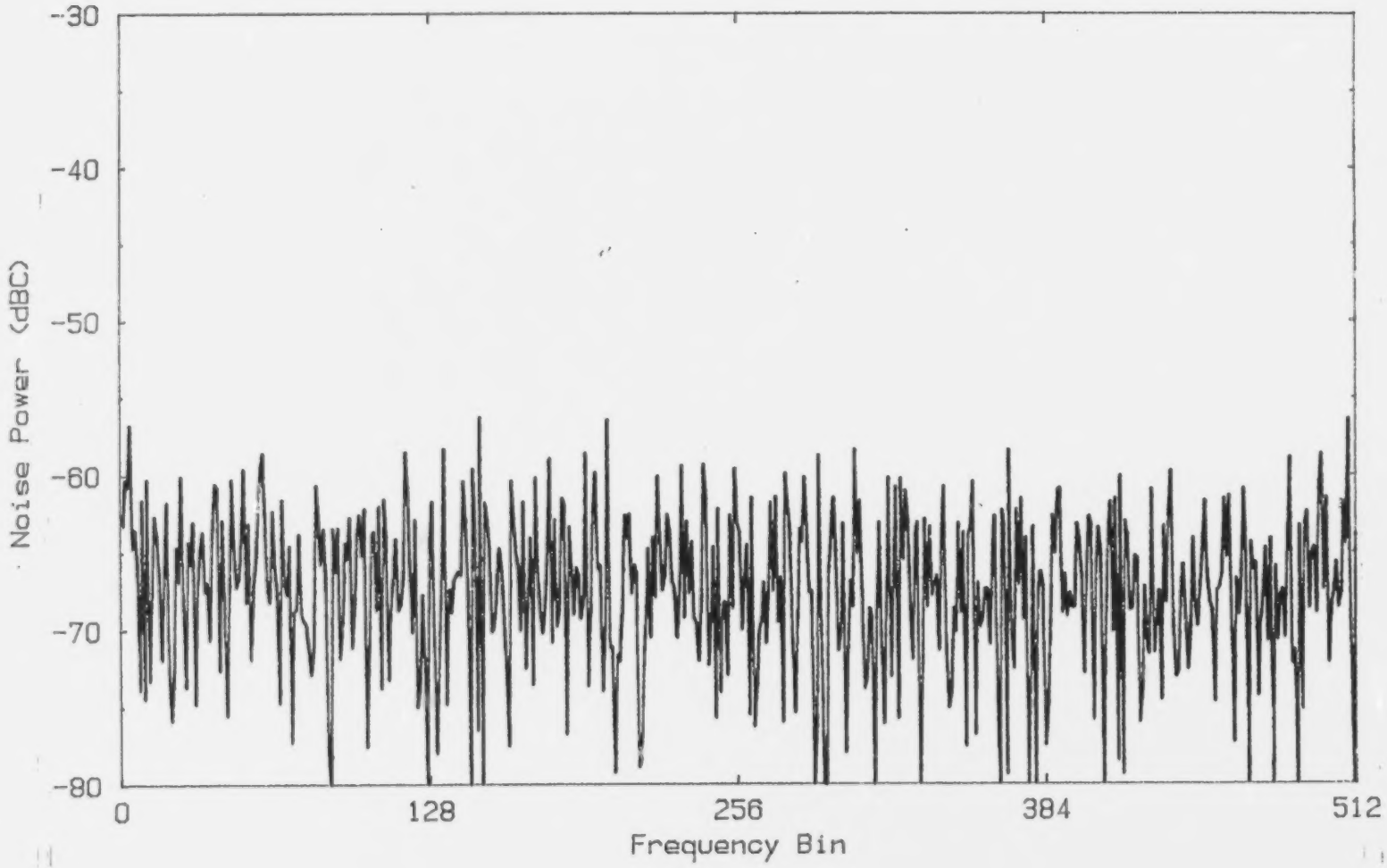


Figure 5.9 Quantizing Noise Power Spectrum (Dither = 10 LSB)

1024
16
64
0

For example, for a bandwidth of 10 MHz and an aperture uncertainty of 2 ps, the estimated noise power is approximately -83 dB relative to the signal power.

5.1.3 Linearity

All non-linear components generate harmonics and intermodulation products, and hence contribute to limiting the spurious-free dynamic range of the system. The general relationship between non-linearity and intermodulation performance that applies to amplifiers and other devices can also be applied to A/D converters.

For the purpose of this analysis, we ignore the effect of differential non-linearity, since the error it introduces is essentially independent at each quantizing level. It is therefore uncorrelated with the input signal (assuming that the signal crosses several quantization levels between samples), and hence contributes to the noise floor rather than to discrete spurious products.

To analyze the effect of integral non-linearity, we assume that the underlying transfer function of the A/D converter (ignoring quantization) is of the form

$$y = x + ax^2 + bx^3$$

where x runs from -1 to +1. The specifications for A/D converters normally give only a single value for integral non-linearity, and hence it is not possible to determine both a and b. We assume $b=0$ when calculating second-order products and $a=0$ when calculating third-order products.

For the above transfer function, the maximum integral non-linearity occurs at the endpoints of the range, and is equal to the coefficient of the distortion term being considered.

5.1.3.1 Second-Order Products

The x^2 term of the transfer function generates the second harmonic of each input tone, and the sum and difference products of pairs of tones. For an input level v, the second harmonic has level $av^2/2$ and the sum and difference products have level av^2.

For example, a non-linearity of 0.1% would give a second harmonic level of 0.0005 or -66 dB for a full-scale sine input.

To measure the sum and difference products, two tones can be applied at a level of $v=0.5$, corresponding to -6 dB (the reduction in level is required to avoid exceeding the full-scale range of the A/D). Each product would have a level of $0.001 * 0.5^2$, or -72 dB relative to full scale.

5.1.3.2 Third-Order Products

The x^3 term of the transfer function generates the third harmonic of each input tone, and the 2f1 ± f2 products of pairs of tones. For an input level v, the third harmonic has level $bv^3/4$ and the two-tone products have level $3bv^3/4$.

A non-linearity of 0.1% would give a third harmonic level of -72 dB for a full-scale input, and two-tone product levels of -80.5 dB for input levels of v=0.5 .

5.1.3.3 Applicability

The above analysis is valid only if the shape of the transfer function is the determining factor in the harmonic and intermodulation performance of the A/D converter. In practice, other factors normally dominate.

For actual devices, the harmonic and intermodulation performance is heavily dependent on the frequency of the input signal, and hence cannot be determined from a linearity value specified at DC (as is normally the case). In addition, the integral linearity is often comparable to the resolution of the converter (e.g., $\pm\frac{1}{2}$ LSB, and hence the concept of an underlying non-linear transfer function is not meaningful.

Figure 5.10 shows the harmonic performance of the CAV-1202, CAV-1205, and CAV-1220 devices over the frequency range 0.01 to 10 MHz, along with the theoretical values corresponding to their specified linearity of 0.0125%. It can be seen that the devices fall short of the theoretical values by 5 to 10 dB even at low frequencies, and by as much as 30 dB at 10 MHz.

The theoretical third-order intermod level for these devices is approximately -98.5 dB, while the actual levels range from -70 dB at low frequencies to -50 dB at 5 MHz.

Based on the above, it appears that the static linearity specification is not useful in predicting harmonic or intermodulation performance.

5.2 Component Performance

Figure 5.11 shows the performance of several state-of-the-art A/D converters, in terms of resolution and maximum sampling rate. Contours of constant signal-to-quantizing-noise ratio are shown for reference.

Note: the values of SNR are based on a 25 kHz channel bandwidth, and assume that the quantizing noise is uncorrelated. This can be ensured if necessary by introducing deliberate dithering.

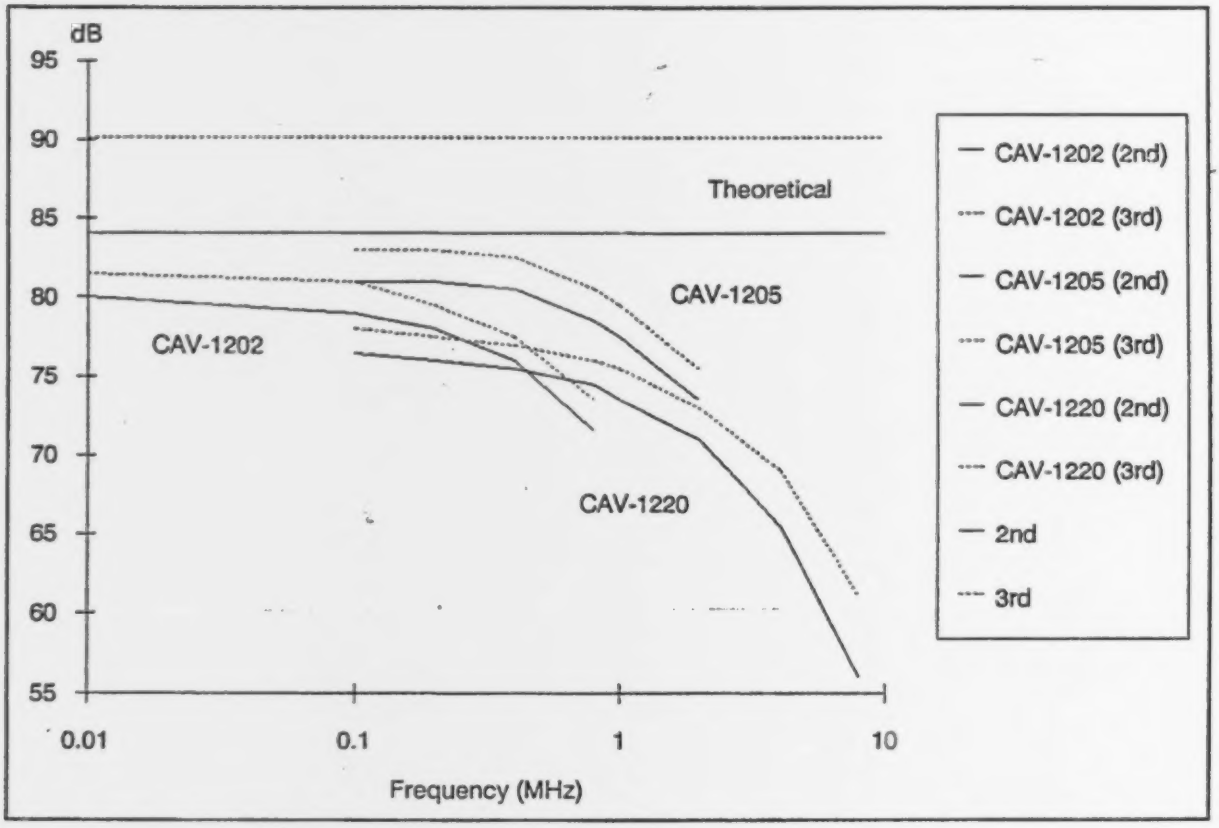


Figure 5.10 A/D Converter Harmonic Distortion

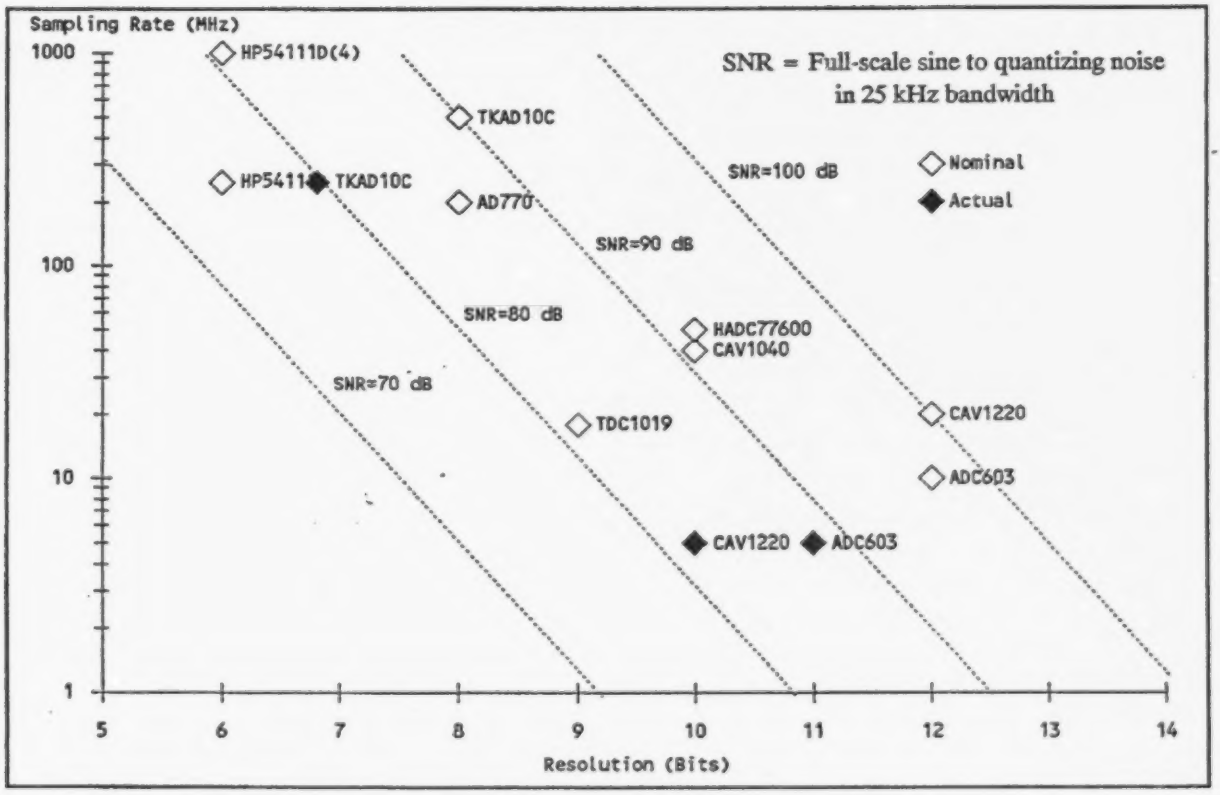


Figure 5.11 A/D Converter Performance

The devices considered provide resolutions of from 6 to 12 bits, with maximum sampling rates of from 10 MHz to 250 MHz. The points marked as "nominal" represent the resolutions and maximum sampling rates of the devices; in practice, the corresponding SNR values are not actually achievable. The points marked "actual" represent operating conditions for which the manufacturers indicate that the corresponding SNR will be achieved.

Of the devices considered, only the Analog Devices CAV-1220 achieves a nominal 100 dB SNR, with a resolution of 12 bits and a sampling rate of 20 MHz. However, its dynamic performance indicates that an actual SNR of only 82 dB can be achieved, using a sampling rate of 5 MHz.

The Burr-Brown ADC603 appears to provide the best actual performance, with an SNR of 88 dB for a sampling rate of 5 MHz. For the case where a high sampling rate is required, the Tektronix TKAD10C provides an actual SNR of 80 dB at 250 MHz.

All of the devices are available as commercial products, except for the HP5411D, which is a component of a sampling oscilloscope produced by Hewlett-Packard. The CAV-1220 and CAV-1040 are fully integrated board-level products. The TRW TDC1019 is included for reference, being the device used in the existing DAR-4000 receiver.

The HP5411D is shown twice, at 250 MHz and at 1 GHz. The latter represents four separate devices operating interleaved, which is the configuration actually used in the sampling oscilloscope. Similarly, the Tektronix TKAD10C consists of a pair of interleaved converters, although fabricated on a single chip. The same technique can be used with any of the devices to increase the sampling rate, as long as suitable sample-and-hold buffering is provided.

5.3 Implementation Considerations

A variety of implementation considerations must be dealt with appropriately to achieve the performance of which a given A/D converter is capable. These include aspects of both circuit design and physical construction.

The implementation factors that are the most critical are determined by the basic parameters of the conversion process: the input bandwidth, the sampling rate, the input level, and the required accuracy.

The analog signal must be presented at the input of the A/D converter at the appropriate voltage and impedance levels. For high-frequency signals, techniques normally associated with RF processing (e.g., constant-impedance transmission lines) may be required.

The sampling clock must be sufficiently stable to avoid excessive degradation of the sampling aperture uncertainty. This translates into a requirement on the phase noise of the clock. For example, at a sampling frequency of 10 MHz, an aperture uncertainty of 2 ps corresponds to a phase jitter of $1.26 * 10^{-4}$ radians and an integrated phase noise level of -78 dBc.

It is crucial that the sample-and-hold device and any preceding circuitry have sufficiently wide frequency response to accommodate the input signal. This is particularly important where intentional aliasing is used to down-convert a bandpass signal, as the signal frequency may be several times the sampling frequency. It is also an area in which published specifications (e.g., for static accuracy) can be highly misleading if interpreted inappropriately.

Any noise sources that contribute to the input signal as seen by the A/D converter must be kept to a level that does not degrade performance excessively. Three broad types of noise can be considered:

1) Low-frequency noise, including DC drift

2) Wideband (uncorrelated) noise

3) Narrow-band noise

Low-frequency noise (e.g., line frequency harmonics), and particularly DC drift, is often the most difficult to deal with. For the cases considered here, however, this type of noise is not a concern, as the frequencies of interest do not extend below several hundred kHz.

It is normally sufficient that the rms level of wideband noise be somewhat below the level of the quantizing noise (typically ± 1/2 LSB). This is not a particularly stringent requirement for the present cases, where the A/D resolution ranges from about 6 to 12 bits. For an input range of ±1 V, the corresponding quantizing noise level is from 0.25 mV to 15 mV. As discussed in section 5.1.1, uncorrelated noise of this magnitude can actually be helpful in some situations, as it can decorrelate the quantizing noise and hence spread its power uniformly across the frequency range covered.

Narrow-band noise within the frequency range of interest is the most critical for this application. Any such noise components should be at least 90 dB below the maximum input level to the A/D converter. This requires highly effective shielding of any noise sources, and careful decoupling of common power supplies.

Proper physical layout and construction is essential for a high-performance A/D conversion subsystem, if problems of ground noise, coupling of interference from the digital circuitry, etc. are to be avoided. If possible, it is preferable to employ an integrated (e.g., board-level) product, typically produced by the manufacturer of the basic A/D converter, rather than the raw device. This ensures that the support

circuitry and the physical layout and construction are appropriate, and reduces the implementation problem essentially to providing a suitable input signal, sampling clock, and power supply, and to accepting and processing the digitized samples.

6.0 DIGITAL PROCESSING

The basic digital processing requirement is to estimate the received power in each of a set of channels, typically 25 kHz wide but potentially as narrow as 100 Hz. It is assumed that FFT processing will be used as the basic spectral estimation technique.

The overall processing flow is as follows:

1) Acquire a block of samples from the A/D conversion subsystem.
2) Multiply the samples by a predefined windowing function. This is required to limit the spectral leakage into frequency bins other than those in the immediate vicinity of a received signal.
3) Perform an FFT of the windowed block.
4) Calculate the squared magnitude of each spectral component.
5) If desired, average the values obtained from a number of successive blocks for each frequency bin, to reduce the variance due to noise.
6) Compare the value for each bin against a specified threshold, to determine the presence or absence of received signals.

6.1 Design Relationships

The critical performance parameter for the digital processing function is the computation rate required, which is determined primarily by the desired sampling rate and frequency resolution. This parameter is most likely to determine whether a given architecture is feasible to implement given the current state of the technology.

Other parameters of interest are the block size that must be accomodated, which is again a function of the sampling rate and the frequency resolution, and the numerical precision required, which is a function of the desired dynamic range.

6.1.1 Windowing

For a signal whose frequency is an exact multiple of the FFT frequency resolution (the reciprocal of the observation time), the FFT output is zero in all bins except the one corresponding to the signal frequency. For other signal frequencies, however, the FFT output has an envelope of the form $\sin(N\theta/2)/\sin(\theta/2)$. This can result in the appearance of spurious signals at levels as high as -13 dB with respect to an actual signal.

The level of these spurious signals, or sidelobes, can be reduced by multiplying the data record by a windowing function. However, this aiso has the effect of broaden-

ing the desired response to a signal at given frequency. To achieve the desired channel selectivity, the FFT bin size must therefore be substantially smaller than the channel bandwidth.

Figure 6.1 shows the "Minimum 4-Term Blackman-Harris" windowing function [1], which provides sidelobe supression of greater than 90 dB and is generally recommended for use where spurious responses must be minimized. Figure 6.2 shows the central portion of the response envelope for this function. It can be seen that the response to a signal is significant within a range of approximately 8 bins centred on the signal frequency. To provide the desired channel selectivity, therefore, the FFT bin size must be no greater than 1/8 the channel bandwidth. This factor will be assumed in the computational analysis below.

6.1.2 Computational Requirements

A sampling frequency fs results in spectral components covering the range 0 to fs/2. (Since we are interested only in power, the negative and positive frequencies can be combined.) To provide a basic frequency resolution of fr, an observation time of 1/fr is required, giving a block size of N = fs/fr. We assume that fs and fr are chosen to make N a power of 2.

The following computation is required for each block:

1) Windowing: N multiplications
2) FFT: $2N\log_2 N$ multiplications and additions
3) Squared Magnitude: N multiplications, N/2 additions
4) Averaging: N/2 multiplications and additions (assumes exponential averaging)

This gives a total of $2N(\log_2 N + 1.25)$ multiplications and $2N(\log_2 N + 0.5)$ additions, both real operations.

Note: a radix-2 FFT is assumed, requiring $N/2 \log_2 N$ complex = $2N\log_2 N$ real multiplications and $N\log_2 N$ complex = $2N\log_2 N$ real additions for an N-point complex transform. Since our input signal is real, however, the computation could be reduced by performing an N/2-point complex transform, with the appropriate rearrangement of the input and output data.

For simplicity, we will assume a computation requirement of $4N\log_2 N$ operations. This weighs multiplications and additions equally, as is the case for most current processors. In practice, overhead operations are likely to increase the overall processing time by from 50% to 100%.

For example, the TMS320C25, rated at 10 MIPS, could be expected to require 4.1 ms to perform a 1024-point FFT (4*1024*10=40960 operations). In practice, it has been measured at 7.2 ms, or about 75% longer than calculated.

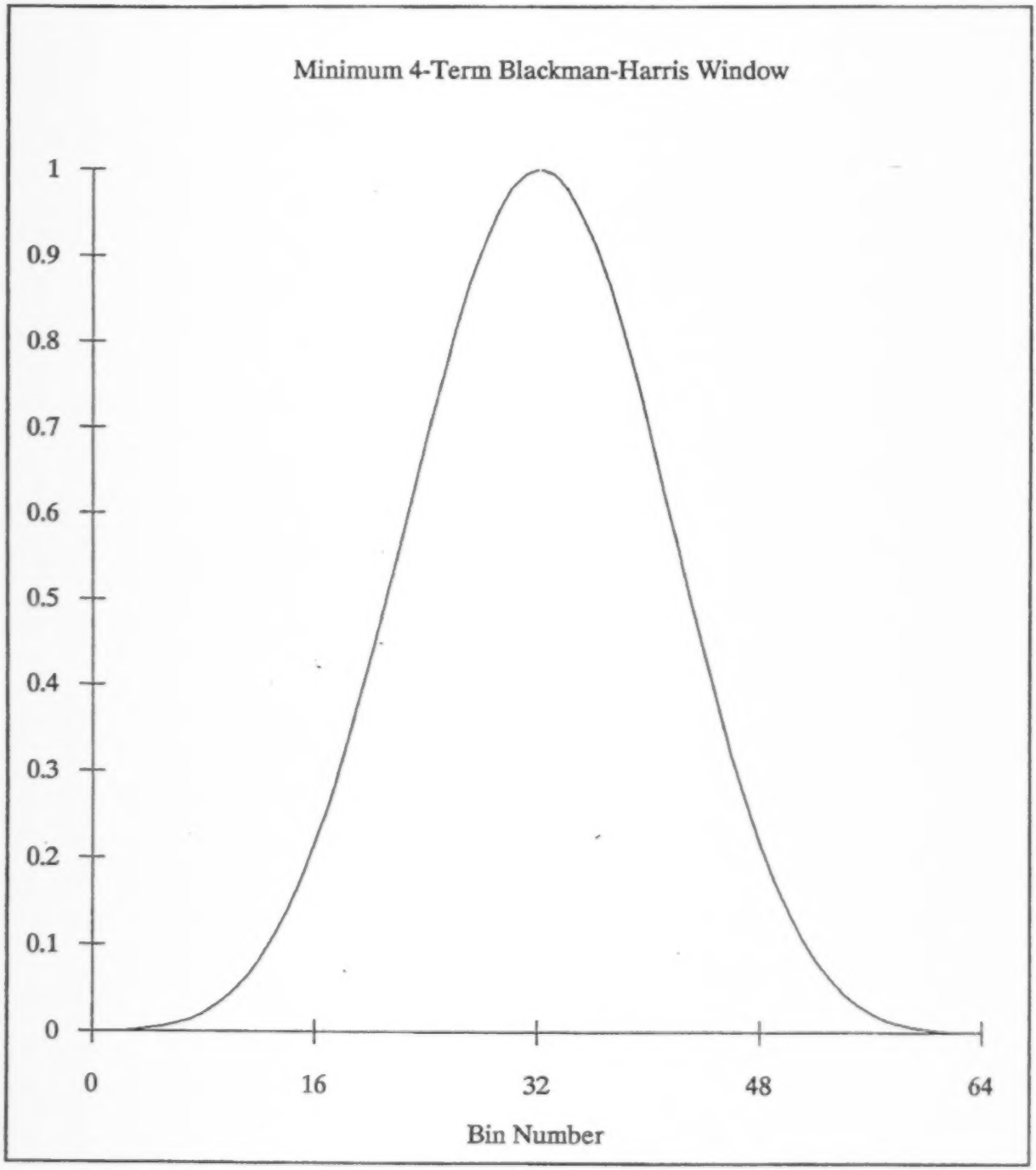


Figure 6.1 Window Function

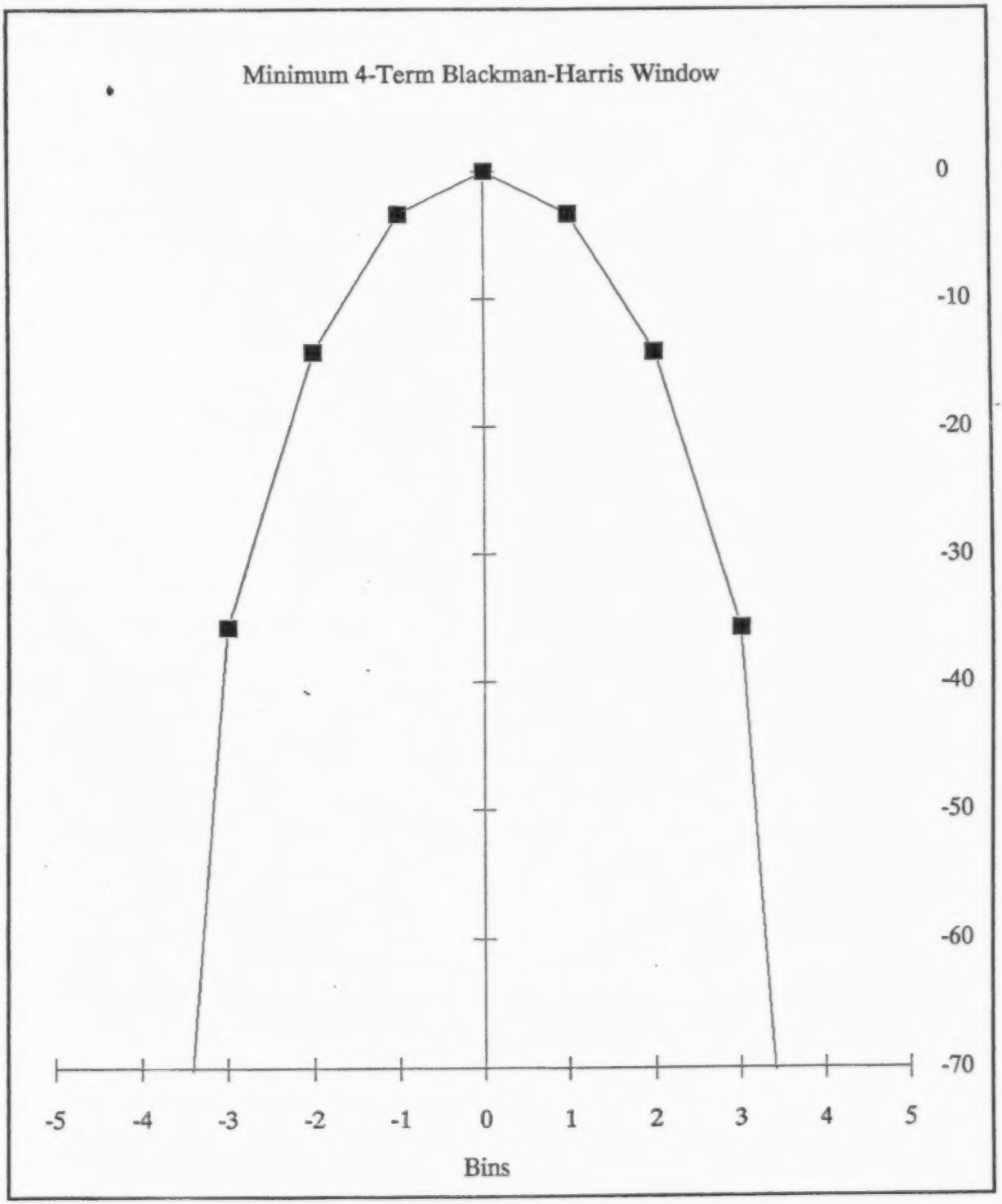


Figure 6.2 Window Spectral Response

6.1.3 Block Size

We have defined architectures using sampling rates of approximately 250 MHz (RF), 20 MHz (Wide-IF), 6.4 MHz (Mid-IF), and 819.2 kHz (Narrow-IF). For channel widths of 25 kHz and 100 Hz, and allowing 8 FFT bins per channel, the following block sizes are required:

Architecture	fs	25 kHz	100 Hz
RF	250 MHz	80,000	20,000,000
Wide-IF	20 MHz	6,400	1,600,000
Mid-IF	6.4 MHz	2,048	512,000
Narrow-IF	819.2 kHz	262	65,536

The block sizes required for 100 Hz channels with the first three architectures are not feasible. In addition, it is not intended to use the Narrow-IF architecture with 25 kHz channels, as it does not provide adequate scanning speed.

It is desirable for the block size to be a power of 2. This can be achieved by adjusting the sampling rates for the RF and Wide-IF architectures.

Taking the above into account, the basic system parameters become as follows:

Architecture	fs (MHz)	25 kHz	100 Hz
RF	204.8	65,536	N/A
Wide-IF	25.6	8,192	N/A
Mid-IF	6.4	2,048	N/A
Narrow-IF	0.8192	N/A	65,536

6.1.4 Processing Speed

For continuous processing, the computation for a block must be performed within the time required to acquire the next block. The required processing speed is therefore $R = 4N\log_2 N/(N/fs) = 4fs\log_2 N$ operations/sec. For the architectures considered, this gives:

Architecture	fs (MHz)	N	R (MOPS)
RF	204.8	65,536	13,107
Wide-IF	25.6	8,192	1,331
Mid-IF	6.4	2,048	282
Narrow-IF	0.8192	65,536	52

Only the Mid-IF and Narrow-IF cases are feasible to implement. Even these are beyond the capacity of a single current general-purpose DSP microprocessor, the fastest of which (Motorola DSP96000) is rated at a maximum of 40 MOPS.

The processing requirements for the RF and Wide-IF architectures can be reduced somewhat by making use of the fact that it is not essential to process continuously, as long as each channel is observed at least once every 10 ms. For the RF architecture, where all channels are observed simultaneously, this gives a required processing speed of $R = 4N\log_2 N/0.01 = 419$ MOPS. It is conceivable that this could be achieved with multiple processors (perhaps 16).

For the Wide-IF architecture, a bandwidth of approximately $fs/3 = 8.5$ MHz would be observed on each block, and 7 blocks would be required to cover the full 30 to 88 MHz band. This would allow 1.43 ms for each block, and would require a processing speed of $R = 4N\log_2 N/0.00143 = 298$ MOPS. This is similar to the requirement for the Mid-IF architecture.

The sampling rate for the Mid-IF architecture was derived in section 3.5.3 to be the minimum for which continuous processing would yield a channel observation rate of 100 Hz.

The sampling rate of the Narrow-IF architecture was derived in section 3.5.4 to correspond to an FFT bin size of 12.5 Hz and an FFT length of 2^{16}. The processing requirement could be reduced by reducing the FFT length (and hence the sampling rate and observation bandwidth).

6.2 Component Performance

There are three main components to be considered for the digital processing function: the processor itself, and the associated program and data memory devices.

6.2.1 Program Memory

The program for the digital processor is likely to be stored in external PROM or EPROM devices. The program size will probably not exceed a few thousand bytes. An access time of approximately 25 ns may be required to support the highest-speed processors.

There should be no difficulty in obtaining devices with the required speed and capacity.

6.2.2 Data Memory

On the order of a megabyte of RAM may be required as data memory. For example, a block of 65536 32-bit samples occupies 256 kB. Space for at least two blocks is required, to allow processing to proceed in parallel with data acquisition.

The memory is accessed in two ways: by the digital processor, and by the A/D conversion subsystem. An access time of 25 ns should be sufficient for the processor, allowing the use of relatively low-cost and high-density (e.g., 32 kbyte) devices. This access time is also compatible with the A/D sampling rates for the IF architectures. However, the RF architecture would require memory with an access time of about 5 ns. While such devices are available, they are likely to be of low capacity (e.g., a few kbits). To allow the use of larger and slower devices, the memory could be implemented with a large word length (e.g., 128 bits), with multiple samples being accessed simultaneously.

6.2.3 Processor

Figure 6.3 shows the rated processing speed of several candidate processors, along with bechmark timings for a 1024-point complex FFT. The relationship derived in section 6.1.2 is shown for reference.

The processing speed is given in millions of operations per second, or MOPS. Some of the processors are capable of executing multiple instructions simultaneously (e.g., a multiplication and an addition), and hence the MOPS rating is greater than the MIPS (millions of instructions per second) rating would be. In practice, the rated MOPS value can be achieved only under circumstances that allow perfect overlapping of parallel instruction sequences.

The devices shown are general-purpose processors except for the TRW TMC2310, which is specifically intended for performing the FFT. The TMC2310 is rated as performing a 1024-point complex FFT (including windowing) in 514 μs, which is a factor of 4 to 5 times less than the best general-purpose processors. The MOPS value shown is derived from the relationship of section 6.1.2.

The TMC2310 is limited to a maximum FFT size of 1024 complex points. Other processors, such as the TMS320C30, can perform FFTs of any practical length.

The TMC2310 implements 16-bit resolution in a 19-bit block floating point format. This provides an instantaneous dynamic range in excess of 96 dB, and an overall dynamic range of approximately 115 dB. The TMS320C30 implements 24-bit resolution in a 32-bit floating point format, giving an instantaneous dynamic range of approximately 144 dB and an effectively infinite overall dynamic range.

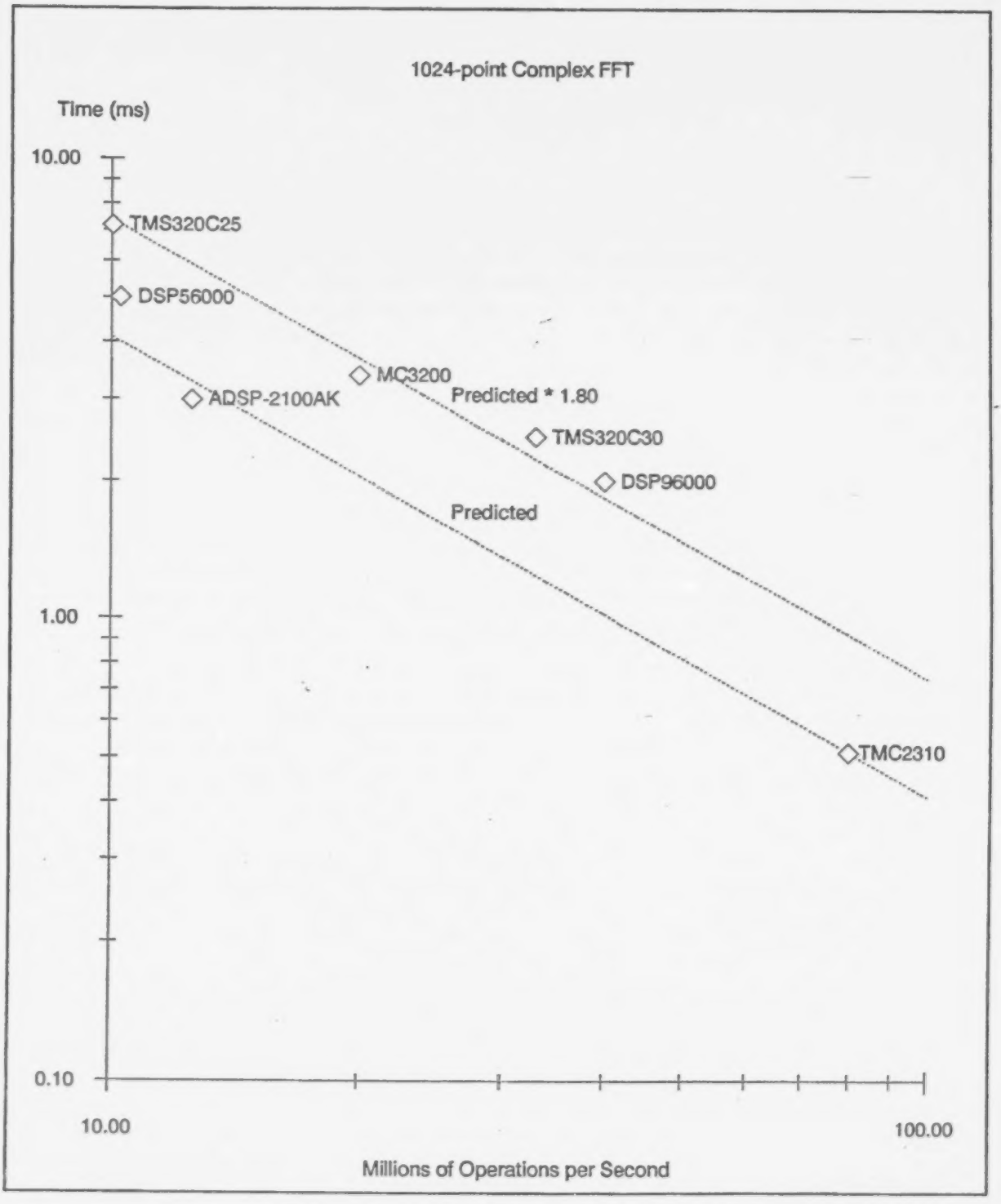


Figure 6.3 Digital Signal Processor Performance

7.0 SYSTEM SELECTION

7.1 Architecture Evaluation

Three primary architectures have been defined, representing full-band sampling at RF and partial-band sampling at two IF bandwidths. A secondary architecture has been defined to support channel bandwidths as small as 100 Hz.

The basic parameters of interest in evaluating the candidate architectures are the channel observation rate, the dynamic range of the analog front end and of the digitization process, and the processing capacity required. These are summarized in Table 7.1 . Note: the channel SNR is derived from the ideal quantization SNR by assuming that the quantization error is uniformly distributed over the observation bandwidth. This is more realistic than assuming it to be uniformly distributed over the entire sampling bandwidth.

The RF architecture has the potential for the best performance, both in dynamic range and in channel observation rate. However, the achievable dynamic range is limited by quantization error to about 84 dB. (This assumes ideal quantization; the performance of a practical A/D converter is likely to be about 6 dB worse than ideal, or 78 dB.) The actual channel observation rate would be limited by the achievable digital processing performance.

The Wide-IF architecture has a slightly poorer potential dynamic range, and a potential channel observation rate one-seventh that of the RF architecture. The achievable dynamic range is limited by A/D converter performance to 87 dB in the ideal case or about 81 dB in practice. However, the sampling rate is just above the current limit for 12-bit A/D converters. It can be anticipated that 12-bit converters for this rate will become available in the near future. This would raise the dynamic range to 99 dB in the ideal case or about 93 dB in practice. At this level, the dynamic range due to quantization would be similar to that due to the analog front end. The channel observation rate would be limited by the achievable digital processing performance.

The Mid-IF architecture has the same potential dynamic range as the Wide-IF. The channel observation rate has been deliberately chosen to be the minimum acceptable. The achievable A/D dynamic range is similar to that of the front-end, about 93 dB, in the ideal case; about 87 dB might be achieved in practice. The digital processing performance required to achieve the target channel observation rate is demanding, but feasible.

The dynamic range of the Narrow-IF architecture is limited by the analog front-end to about 94 dB. The required digital processing performance could be provided by about two of the current DSP microprocessors working in parallel.

	RF	Wide-IF	Mid-IF	Narrow-IF
Sampling Rate	204.8 MHz	25.6 MHz	6.4 MHz	819.2 kHz
FFT Length	65536	8192	2048	65536
Observation Time	320 us	320 us	320 us	80 ms
FFT Resolution	3.125 kHz	3.125 kHz	3.125 kHz	12.5 Hz
Observation Bandwidth	68.0 MHz	8.5 MHz	2.0 MHz	273.1 kHz
Channel Bandwidth	25.0 kHz	25.0 kHz	25.0 kHz	100.0 Hz
Channels Observed	2720	340	80	2731
Bands in 58 MHz	1	7	29	213
Revisit Time	320 us	2240 us	9280 us	17 s
Revisit Rate	3125 Hz	446 Hz	108 Hz	0.059 Hz
Quantization Bits	8	10	12	12
Quantization SNR (Ideal)	49.9 dB	62.0 dB	74.0 dB	74.0 dB
Channel SNR (Ideal)	84.3 dB	87.3 dB	93.0 dB	108.4 dB
Analog DRs	96.6 dB	93.7 dB	93.7 dB	93.7 dB
Processing Requirement	13107 MOPS	1331 MOPS	282 MOPS	52 MOPS

Table 7.1 Architecture Evaluation Parameters

7.2 Architecture Selection

Because digital processing performance is the limiting factor in determining the achievable channel observation rate, there is no advantage from this standpoint in digitizing a wider band than can be processed continuously. As FFT computation increases faster than linearly with block size, the achievable channel observation rate actually decreases with increasing sampling frequency for a given processing capacity. The best performance is obtained by sampling at the widest bandwidth that can be processed continuously. With the current technology, this bandwidth is similar to that proposed for the Mid-IF architecture. Coincidentally, this is also the minimum bandwidth that allows the overall system performance target to be met.

Because A/D performance is the limiting factor in determining the achievable dynamic range, the Mid-IF architecture, though worse than the RF architecture from the standpoint of the analog front end, actually provides the best system performance.

For these reasons, the Mid-IF architecture appears to be optimal, and will be assumed in the subsequent analysis. To allow 100 Hz channels to be resolved, the overall system will be assumed to include the Narrow-IF architecture as well.

7.3 Processing Architecture

The highest-performance processor that has been considered is the TRW TMC2310. This device is well suited to performing the basic FFT operation. However, an additional general-purpose processor would be required for other data manipulation and analysis.

The largest FFT block size supported by the TMC2310 is 1024 complex points. The block size of 2048 selected for the Mid-IF architecture can be accomodated by storing alternate samples into the real and imaginary components of the input array, and performing an additional processing step on the output array.

The TMC2310 requires 514 μs to perform the 1024-point FFT. There is a total of 10 ms / 29 = 345 μs available for processing each block, and hence two TMC2310 devices operating in parallel on alternate blocks are required.

The following functions must be performed on the output of the TMC2310:

1) Convert the array into the DFT of the 2048-point real data sequence. This requires one complex multiply and three complex additions, or a total of 12 real operations, per bin.

2) Compute the power for each bin. This requires two real multiplies and one add, or a total of 3 operations, per bin.

3) Perform time averaging if desired. This requires one multiply and one add, or a total of 2 operations, per bin.

4) Compare the power to a detection threshold. This requires one operation per bin.

The above functions constitute a total of 18 operations per bin. Note that only the bins in the observation bandwidth need be processed: for the 2 MHz bandwidth assumed for Mid-IF architecture, this corresponds to 2 MHz / 3.125 kHz = 640 bins. The required processing speed is then 640*18/345 = 33.4 MOPS, which is close to the peak capacity of one TMS320C30 device. In practice, two devices operating in parallel on alternate blocks should be sufficient.

The above suggest the use of two identical processing modules, each consisting of a TMC2310 front-end FFT processor and a TMS320C30 back-end analysis processor, operating on alternate blocks. This architecture has the advantage of being easily expanded to handle higher sampling rates by adding further interleaved modules.

An overall host processor would also be required, to control the processing modules and to communicate with the user. A standard microprocessor (e.g., 80x86 or 680x0) should be suitable.

As proposed, the analysis of 100 Hz channels requires an FFT block size of 65536 (real). This can be accommodated by processing sequential 2048-point blocks (packed into 1024 complex points, as above) in the TMC2310, and combining these in the TMS320C30 to synthesize the full-length FFT. This effectively implements the first 10 levels of the FFT lattice in the TMC2310, and the remaining 5 levels in the TMS320C30.

The additional computation required in the TMS320C30 is 4*5 = 20 real operations per bin. Note that in this case, all bins must be processed. The total computation, assuming an observation bandwidth of 273 kHz or 21848 bins, is then 18*21848 + 20*65536 = 1,703,984 operations. As the observation time is 80 ms, the computation rate is 21.3 MOPS. This is again within the capacity of two TMS320C30s operating on alternate blocks. The TMC2310s are very lightly loaded in this case.

8.0 PERFORMANCE ANALYSIS

8.1 Signal Processing Performance

The signal processing performance characteristics of the proposed architecture, as derived above, are summarized here for convenience.

8.1.1 Dynamic Range

The receiver subsystems provide the following instantaneous spurious-free dynamic range performance:

	25 kHz	100 Hz
Front end	94 dB	94 dB
A/D converter	87 dB	102 dB
Digital processing	96 dB	96 dB

For 25 kHz channels, the A/D converter limits the overall dynamic range to approximately 87 dB, while for 100 Hz channels the analog front end limits it to approximately 94 dB.

Note: the A/D converter figures assume a degradation of 6 dB from theoretical performance. For an ideal 12-bit converter, the overall dynamic range for 25 kHz channels would be 93 dB.

8.1.2 Frequency Range

The proposed system covers the 30-88 MHz range. As RF digitization has not been chosen, it is probably desirable to use preselector filters to divide the input range into sub-octave bands. This would avoid spurious second-order responses, and would also facilitate extending the coverage to lower frequencies.

8.1.3 Frequency Resolution

The proposed system provides basic frequency resolutions of 3.125 kHz and 12.5 Hz. Sidelobe rejection of approximately 90 dB can be achieved for channel widths of 8 bins, corresponding to 25 kHz and 100 Hz.

Frequency resolution of a multiple of the basic resolution can be achieved by summing over the appropriate number of bins in the analysis or host processor.

8.1.4 Observation Rate

With a channel width of 25 kHz, each channel in the full 30-88 MHz band can be observed 100 times per second. This is equivalent to a scanning rate of 232,000 channels per second.

Approximately 17 seconds is required to observe the entire band with a channel width of 100 Hz. This is equivalent to a scanning rate of 34,000 channels per second.

8.2 Probabilistic Performance

8.2.1 Probability of Interception

The primary target signal of interest has been defined as having a 25 kHz bandwidth and a dwell time at any frequency of at least 10 ms. As the proposed system can observe the entire 30-88 MHz band at a 100 Hz rate, the probability of interception for this signal is 100%.

8.2.2 Detection Criterion

Detection of a target signal would be based upon the spectral magnitude in a given FFT bin exceeding a specified threshold, either on a single observation or on the average of several consecutive observations. The threshold would be chosen for the given signal environment to achieve the best trade-off between probability of detection and probability of false alarm. Depending on the environment, the optimum threshold could vary across the coverage band.

In practice, it would likely be necessary to perform additional processing and filtering on the raw detection information, such as signalling changes in detection status for a given bin, excluding portions of the coverage range from consideration, etc.

8.2.3 Probability of Detection and of False Alarm

As indicated above, the probability of interception for the signals of interest is 100%, and hence the probability of detection (Pd) and the probability of detection given interception (Pd/I) are equivalent.

In the absence of a target signal, the magnitude of a given FFT bin can be assumed to have a Rayleigh distribution, corresponding to envelope detection of Gaussian noise. With a signal present, the distribution is Rician, which when the signal is large compared to the noise approaches a Gaussian distribution with mean equal to the signal level and standard deviation equal to $1/\sqrt{2}$ times the rms noise level.

The probability of false alarm is then the probability that the Rayleigh-distributed noise exceeds the threshold, while the probability of detection is the probability that the Rice-distributed signal plus noise falls below the threshold. These are standard results in detection theory.

8.2.4 Effect of Averaging

The variation in the measured levels due to noise can be reduced by averaging multiple measurements. For the case of a continuous signal, averaging N measurements leaves the signal level constant while reducing the standard deviation due to

noise by $1/\sqrt{N}$ (assuming that the noise samples are independent). Given sufficient stability in the measurement equipment, this allows the detection of signals at well below 0 dB SNR.

For the case of an intermittent signal such as a frequency hopper, however, averaging can reduce the effective level of the signal and hence degrade detection performance. For example, if the hopping period is equal to the measurement interval, only one measurement of the N being averaged would be expected to include the signal for any bin which the signal occupied during a given averaging period. The effect of the signal would therefore be reduced by 1/N. As the standard deviation due to noise is reduced only by $1/\sqrt{N}$, the signal becomes harder to distinguish from the noise.

Optimal averaging is achieved with the longest averaging period for which the signal is guaranteed to be continuously present. Assuming that there is no synchronization between the averaging frames and the signal activity, this is equal to one-half the minimum signal duration. In this case, if the signal appears part way through a given averaging frame, it is assured to be present throughout the next frame.

Note: this seems to imply that it would be necessary to observe a hopper of 10 ms dwell time at at least 200 Hz, rather that at 100 Hz as proposed, to ensure that the signal was active throughout the duration of at least one measurement. This would be the case if the signal were observed continuously between measurements. However, as the actual observation time is much less (e.g., 320 μs), it is sufficient for the observation interval to be slightly less than the dwell time (specifically, the dwell time less the observation time, or 9.68 ms, corresponding to an observation rate of 103.3 Hz).

9.0 RECOMMENDATIONS

9.1 Implementation Estimates

Table 9.1 presents an estimate of the material and labour costs involved in implementing the receiver system as described in this report. No fee element has been included, as this would depend on the contractual arrangements (e.g., fixed-price vs. per diem rate, customer-furnished equipment, etc.).

The overall project duration would be from 12 to 18 months, depending on the project team structure.

Figure 9.1 shows a block diagram of the system to which the implementation estimate applies. As indicated below, additional control, post-processing, and display functions would be required in a practical system. It is assumed that these would be implemented in an external host processor.

9.2 Further Work

The current report has verified the general feasibility of implementing a receiver system that meets the primary requirement of observing the 30 to 88 MHz band with 25 kHz channel selectivity at a rate of 100 Hz, and has proposed a suitable candidate architecture. However, it has not addressed the issues of how the receiver operation is to be controlled by the operator, or of how the raw data produced by the receiver (e.g., records of signal detections) is to be presented to the operator, analyzed, or otherwise made use of.

Further work on this subject could proceed as follows:

1) Review the fundamental assumptions and performance requirements on which this report is based.

2) Define the control, post-processing, and display capabilities that would be required in a practical receiver system.

3) Revise the proposed receiver architecture as required to be compatible with the results of the above. Note that considerable additional processing capacity could be required to manage the large volume of raw data produced by the receiver.

4) Design, implement, and evaluate a prototype receiver system.

MATERIALS	Quantity	Unit Cost	Total
RF Switches	4	$500	$2,000
Bandpass Filters	5	$500	$2,500
RF Amplifiers	3	$500	$1,500
Mixers	2	$125	$250
Synthesizer 305-363 MHz	1	$10,000	$10,000
Oscillator 286.2 MHz	1	$500	$500
Clock Oscillators	2	$50	$100
Transformer 50:600	1	$100	$100
A/D Converter	1	$5,000	$5,000
TMC2310	2	$500	$1,000
TMS320C30	2	$500	$1,000
RAM			$2,500
Interface and Control Circuitry			$2,500
Chassis, connectors, power supplies			$2,500
Spares and miscellaneous			$5,000
			$36,450
LABOUR	Months	Unit Cost	Total
System Design	2	$9,000	$18,000
Analog Design	2	$9,000	$18,000
Digital Design	4	$9,000	$36,000
Software Design (TMS320)	2	$9,000	$18,000
Mechanical Design	1	$9,000	$9,000
Procurement and Assembly	2	$5,000	$10,000
Software Implementation	3	$9,000	$27,000
Integration and Testing	4	$9,000	$36,000
Documentation	3	$9,000	$27,000
Program Management	2	$12,000	$24,000
			$223,000
SUMMARY			
Materials	$36,450		
Labour	$223,000		
Total	$259,450		

Table 9.1 Implementation Estimates

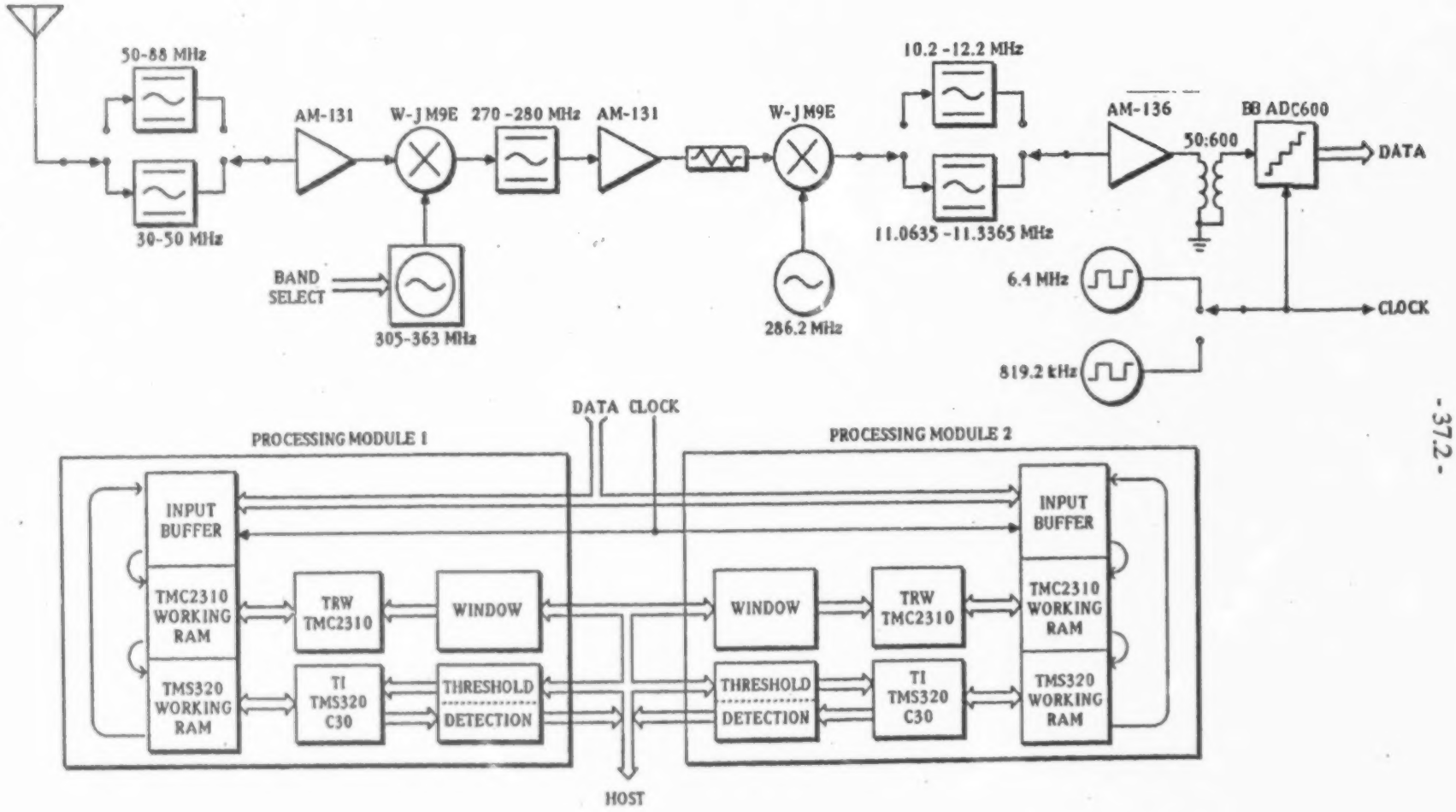


Figure 9.1 Receiver Block Diagram

10.0 REFERENCES

[1] Harris, F.J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Proceedings of the IEEE, Vol. 66, No.1, January 1978, pp 51-83.

UNCLASSIFIED

SECURITY CLASSIFICATION OF FORM
(highest classification of Title, Abstract, Keywords)

DOCUMENT CONTROL DATA

(Security classification of title, body of abstract and indexing annotation must be entered when the overall document is classified)

1. ORIGINATOR (the name and address of the organization preparing the document. Organizations for whom the document was prepared, e.g. Establishment sponsoring a contractor's report, or tasking agency, are entered in section 8.)

Miller Communications Systems Ltd.
300 Legget Drive
Kanata, Ontario, K2K 1Y5

2. SECURITY CLASSIFICATION (overall security classification of the document including special warning terms if applicable)

Unclassified

3. TITLE (the complete document title as indicated on the title page. Its classification should be indicated by the appropriate abbreviation (S,C,R or U) in parentheses after the title.)

Digital Receiver System Study Final Report (U)

4. AUTHORS (Last name, first name, middle initial. If military, show rank, e.g. Doe, Maj. John E.)

Bodie, John B.

5. DATE OF PUBLICATION (month and year of publication of document)

March, 1989

6a. NO. OF PAGES (total containing information. Include Annexes, Appendices, etc.)

77

6b. NO. OF REFS (total cited in document)

1

6. DESCRIPTIVE NOTES (the category of the document, e.g. technical report, technical note or memorandum. If appropriate, enter the type of report, e.g. interim, progress, summary, annual or final. Give the inclusive dates when a specific reporting period is covered.)

Final Report

8. SPONSORING ACTIVITY (the name of the department project office or laboratory sponsoring the research and development. Include the address.)

DREO

9a. PROJECT OR GRANT NO. (if appropriate, the applicable research and development project or grant number under which the document was written. Please specify whether project or grant)

041LK11

9b. CONTRACT NO. (if appropriate, the applicable number under which the document was written)

60ER-7-0003/96

10a. ORIGINATOR'S DOCUMENT NUMBER (the official document number by which the document is identified by the originating activity. This number must be unique to this document.)

DREO-04

10b. OTHER DOCUMENT NOS. (Any other numbers which may be assigned this document either by the originator or by the sponsor)

CONTRACTOR REPORT 89-651

11. DOCUMENT AVAILABILITY (any limitations on further dissemination of the document, other than those imposed by security classification)

- (X) Unlimited distribution
- ( ) Distribution limited to defence departments and defence contractors; further distribution only as approved
- ( ) Distribution limited to defence departments and Canadian defence contractors; further distribution only as approved
- ( ) Distribution limited to government departments and agencies; further distribution only as approved
- ( ) Distribution limited to defence departments; further distribution only as approved
- ( ) Other (please specify):

12. DOCUMENT ANNOUNCEMENT (any limitation to the bibliographic announcement of this document. This will normally correspond to the Document Availabilty (11). However, where further distribution (beyond the audience specified in 11) is possible, a wider announcement audience may be selected.)

UNCLASSIFIED

13. ABSTRACT (a brief and factual summary of the document. It may also appear elsewhere in the body of the document itself. It is h desirable that the abstract of classified documents be unclassified. Each paragraph of the abstract shall begin with an indication of the security classification of the information in the paragraph (unless the document itself is unclassified) represented as (S), (C), (R), or (U). It is not necessary to include here abstracts in both offical languages unless the text is bilingual).

This report examines the factors that determine the performance of hybrid analog/digital wideband Communications ESM surveillance receivers employing conventional electronic signal processing techniques.

A set of receiver architectures is defined, each reflecting a different location of the analog/digital boundary. The feasibility and performance of each architecture is evaluated in the light of the current state of the art in analog and digital processing technology.

The optimal architecture is selected and is analyzed in detail. Estimates are provided of the cost and time required to implement the selected architecture.

14. KEYWORDS, DESCRIPTORS or IDENTIFIERS (technically meaningful terms or short phrases that characterize a document and could be helpful in cataloguing the document. They should be selected so that no security classification is required. Identifiers, such as equipment model designation, trade name, military project code name, geographic location may also be included. If possible keywords should be select from a published thesaurus. e.g. Thesaurus of Engineering and Scientific Terms (TEST) and that thesaurus-identified. If it is not possible to select indexing terms which are Unclassified, the classification of each should be indicated as with the title.)

Radio Receivers
Digital Receivers
Receiver Dynamic Range
Surveillance Receivers
Analog-to-Digital Conversion
FFT Processing
Electronic Support Measures
Electronic Warfare